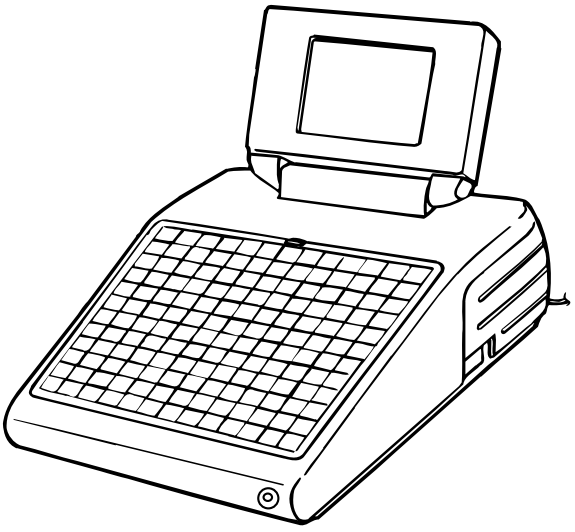
SHARP SERVICE MANUAL

CODE: 00ZERA750VSME



MODEL ER-A750

(For "V" version)

CONTENTS

CHAPTER 1. SPECIFICATIONS 1-1

CHAPTER 2. OPTIONS 2-1

CHAPTER 3. SERVICE PRECAUTION 3-1

CHAPTER 4. SRV RESET (Program Loop Reset) and switch to SRV mode 4-1

CHAPTER 5. MASTER RESET 5-1

CHAPTER 6. DIAGNOSTICS SPECIFICATIONS 6-1

CHAPTER 7. CIRCUIT DESCRIPTION 7-1

CHAPTER 8. CIRCUIT DIAGRAM 8-1

CHAPTER 9. PWB LAYOUT 9-1

PARTS GUIDE

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

This document has been published to be used for after sales service only.
The contents are subject to change without notice.

- There is an erroneous description on JOB# 981-A setting on page 32 of the ER-A750 Programming Manual. Please correct your manual.

<Wrong>

981-A: 1. Tax amount display on screen

1. Tax amount display on screen	931-A	
No	0	★
Yes	4	

<Correct>

981-A: 1. Tax amount display on screen

2. Z report on only display

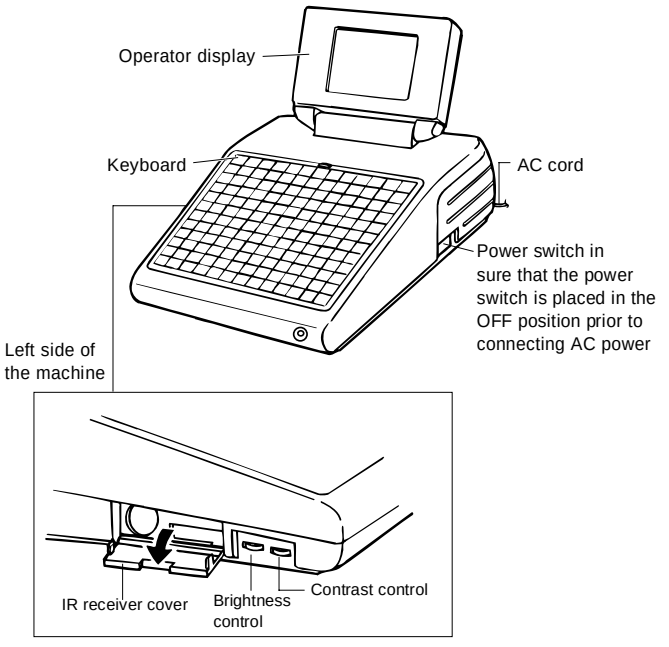
1. Tax amount display on screen	2. Z report on only display	981-A	
No	Disable	0	
	Enable	2	
Yes	Disable	4	★
	Enable	6	

CHAPTER 1. SPECIFICATION

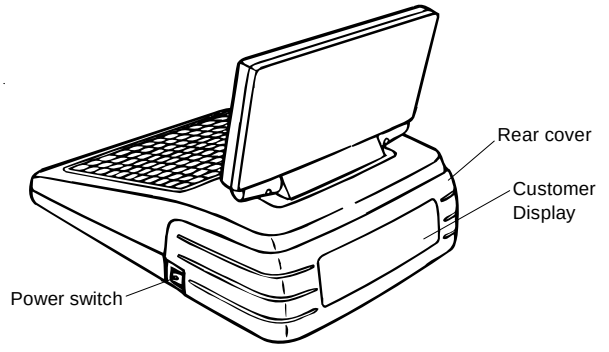
1. Apearance

External view

Front view


Operator display
Keyboard
AC cord
Power switch in sure that the power switch is placed in the OFF position prior to connecting AC power
Left side of the machine
IR receiver cover
Brightness control
Contrast control

Rear view

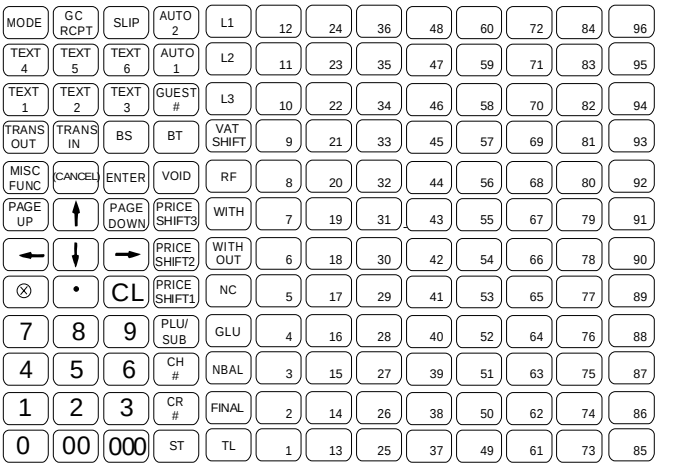


2. Rating

External dimensions	290 (W) × 365 (D) × 262 (H) mm
Weight	5.1 kg
Power source	Official voltage and frequency
Power consumption	Stand-by: 22W Operating: 26W (max.)
Working temperatures	0 to 40°C

3. Keyboard

1) Standard keyboard layout



2) Key top name

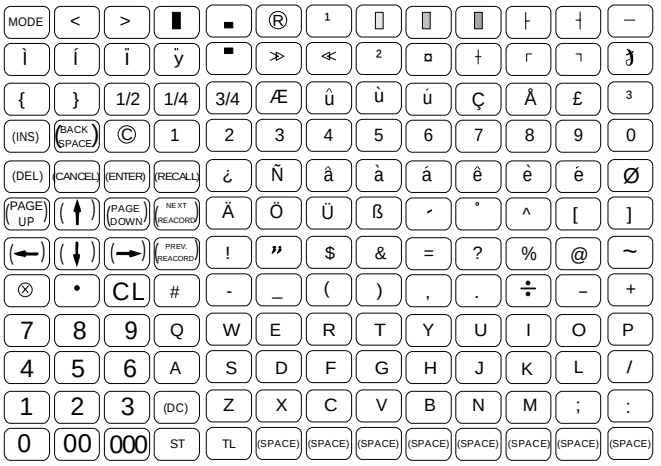
① Standard key top

KEY TOP	DESCRIPTION
0 ~ 9,000, 00	Numeric keys
•	Decimal point key
CL	Clear key
⊗	Multiplication key
VAT SHIFT	Value-added tax shift key
RF	Refund key
VOID	Void key
PLU / SUB	Price lookup / Subdepartment key
1 ~ 96	Direct price look up key
L1 ~ L3	PLU level shift 1 ~ 3 keys
FINAL	Tentative finalization key
MISC FUNC	Miscellaneous function key
MODE	Mode menu key
ENTER	Enter key
AUTO1,2	Automatic sequencing 1 and 2 keys
CR#	Credit menu key
CH#	Check menu key
ST	Subtotal key
TL	Total key
PAGE UP	Page up key
PAGE DOWN	Page down key
→	Cursor right key
←	Cursor left key
↑	Cursor up key
↓	Cursor down key
CANCEL	Cancel key
WITH	With key
WITH OUT	Without key
TEXT1 ~ 6	Direct text 1 ~ 6 keys
PRICE SHIFT 1 ~ 3	Price level shit 1 ~ 3 keys
GC RCPT	Guest check receipt key
GUEST #	Guest number entry key
NC	New check key
GLU	Guest lookup key
NBAL	New balance key
TRANS OUT	Transfer out key
TRANS IN	Transfer in key
SLIP	Slip print key
BS	Bill separation key
BT	Bill totalize / Bill transfer key

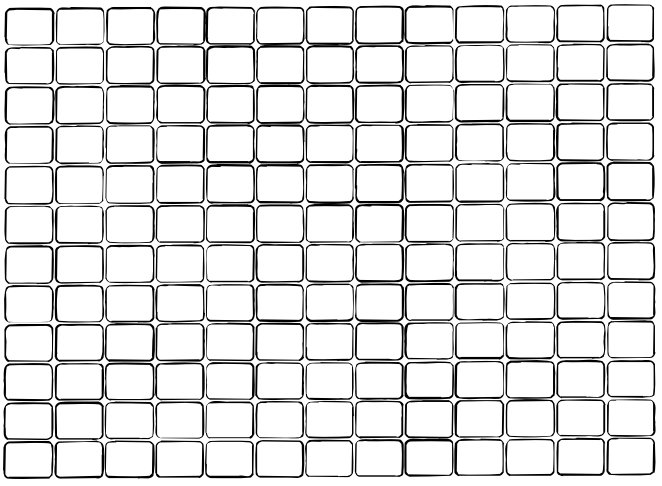
② Optional key top

KEY TOP	DESCRIPTION
97 ~ 135	Direct price look up keys
1 ~ 99	Department keys
%1 ~ %9	Percent 1 ~ 9 keys
⊖1 ~ ⊖9 keys	Discount 1 ~ 9 keys
CR1 ~ CR8	Credit 1 ~ 8 keys
CA2	Cash total 2 key
RA1,RA2	Received on account 1 and 2 keys
PO1,PO2	Paid out 1 and 2 keys
AUTO3 ~ AUTO25	Automatic sequencing 3 ~ 25 keys
CH1 ~ CH4	Check 1 ~ 4 keys
CASH TIP	Cash tip key
TIP PAID	Tip paid key
#	Non-add code entry key
NS	No-sale key
MGR#	Manager code entry key
OPEN TARE	Tare entry Key
REPEAT	Repeat entry key
PERSON#	Person number entry key
IND. PAYMENT	Individual payment key
RCP. SW	Receipt ON / OFF key
SCALE	Scale entry key
TEXT 7 ~ 10	Text 7 ~ 10 keys
EX1 ~ 9	Foreign currency exchange 1 ~ 9 keys
AMT	Amount entry key
DRV NC	New check 2 key (For drive-thruogh)
DRV GLU	Guest look up 2 key (For drive-through)
VAT	Value-added tax key
NON-CASH TIP	Non-cash tip key
1/2	1/2 key
CLERK#	Clerk code entry key
RCPT	Receipt print key
PINT	Pint key
DEPO(+)	Deposit plus entry key
DEPO(–)	Deposit minus entry key
TEXT#	Text number key
EMP#	Employee key
TIME IN	Time in key
SBTL VOID	Subtotal void key
TIME OUT	Time out key
BREAK IN/OUT	Break in/out key
VP	Validation print key
RTN	Return key
DEPT SHIFT 1 ~ 4	Department shift 1 ~ 4 keys
RCPT SHIFT	Receipt shift key
DIFFER ST	Difference subtotal key
C.BILL	Cumulated bill key
GC COPY	Guest check copy key
EX#	Foreign currency exchange menu key
VIP	VIP sale key
H.T.	Hotel transfer key
CLK1 ~ 10	Clerk entry 1 ~ 10 keys
CHECK PRINT	Check print key

3) Text programming key sheet layout



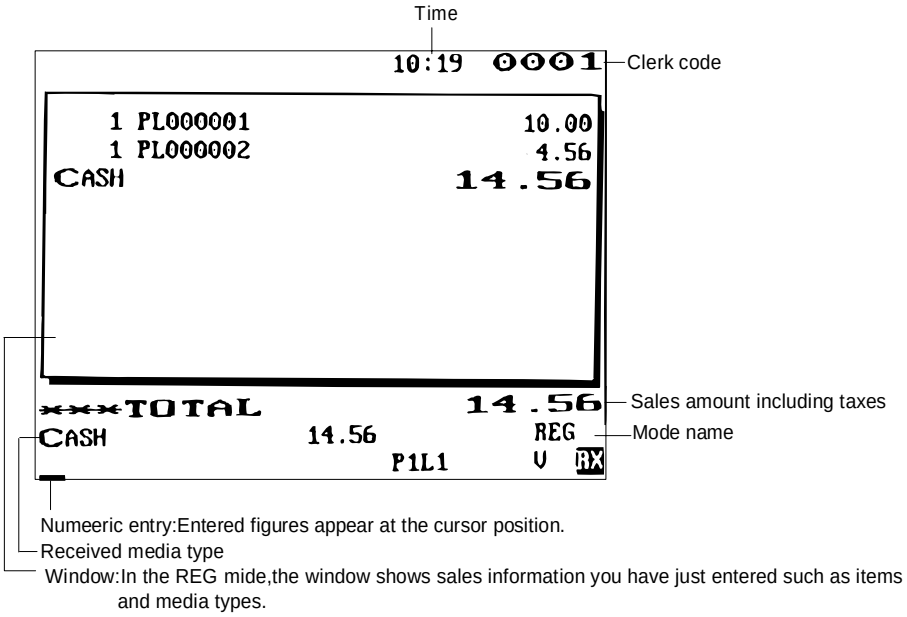
4) Blank key sheet layout



3. Display

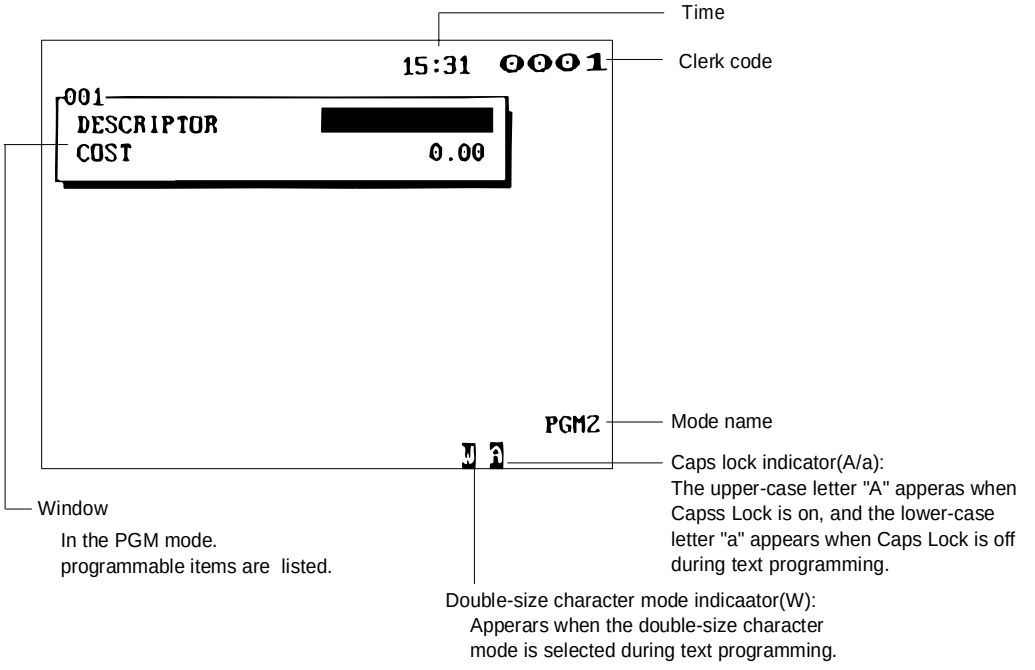
1) Operator display

- Screen example 1 (REG mode)


Time
10:19 0001
Clerk code
1 PL000001 10.00
1 PL000002 4.56
CASH 14.56
****TOTAL 14.56
Sales amount including taxes
CASH 14.56 REG
Mode name
P1L1 V RX
Numeeric entry:Entered figures appear at the cursor position.
Received media type
Window:In the REG mide,the window shows sales information you have just entered such as items and media types.

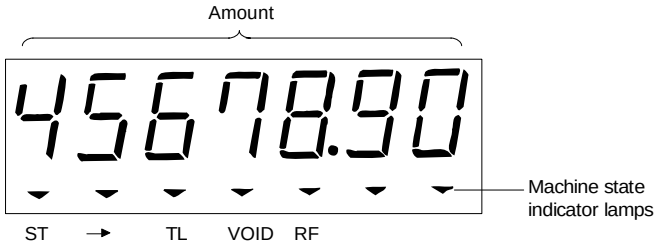
Prive level shift indicator (P1-P3) : Shows the PLU price level currently selected.
PLU level shift indicator (L1-L3) : Shows the PLU level currently selected.
Stock alarm indicator (!) : Appears when the stock of the PLU which you entered is zero or negative.
Department shift status indicator (D1-D4) : Shows the department shift status currently selected.
VAT shift status indicator (V) : Appears when the VAT status is shifted.
Receipt ON/OFF status indicator (R) : Appears when the receipt ON-OFF function signs OFF.
Sentinel mark (X) : Appears in the lower right corner of the screen when the cash in drawer exceeds a programmed sentinel amount.
The sentinel check is performed for the total cash in drawer.

- Screen example 2 (PGM mode)


Time
15:31 0001
Clerk code
001
DESCRIPTOR
COST 0.00
PGM2
Mode name
Caps lock indicator(A/a):
The upper-case letter "A" apperas when Capss Lock is on, and the lower-case letter "a" appears when Caps Lock is off during text programming.
Window
In the PGM mode.
programmable items are listed.
Double-size character mode indicaator(W):
Apperars when the double-size character mode is selected during text programming.

Device type	LCD display
Dot format	320(W) × 240(H) Full dot
Dot size	0.33 × 0.33 mm
Dot space	0.03 mm
Dot color	White
Back color	Dark blue
Weight	180 g

2) Customer display



ST: Lights up when a subtotal is displayed.

→: Lights up when the change due amount appears in the display or when the total sale amount is negative.

TL: Lights up when you finalize a transaction without any amount tendered entry.

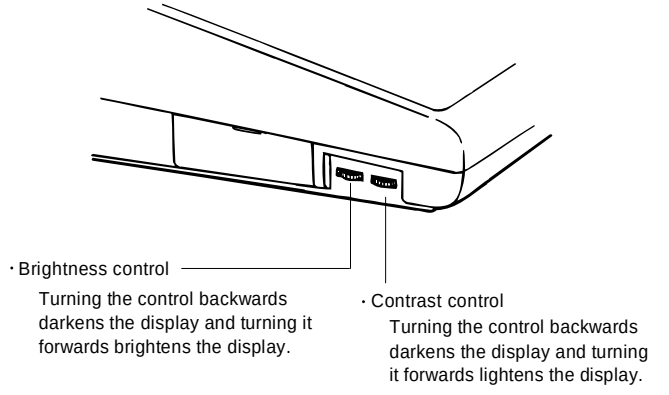
VOID: Lights up when the [VOID] key is pressed or when an item void entry is made.

RF: Lights up when the [RF] key is pressed or when a refund item entry is made.

Device type	7 segment display tube
Number of lines	1 line
Number of positions	7 positions numeric display
Color of display	Green
Character size	13(H) × 6(W) mm

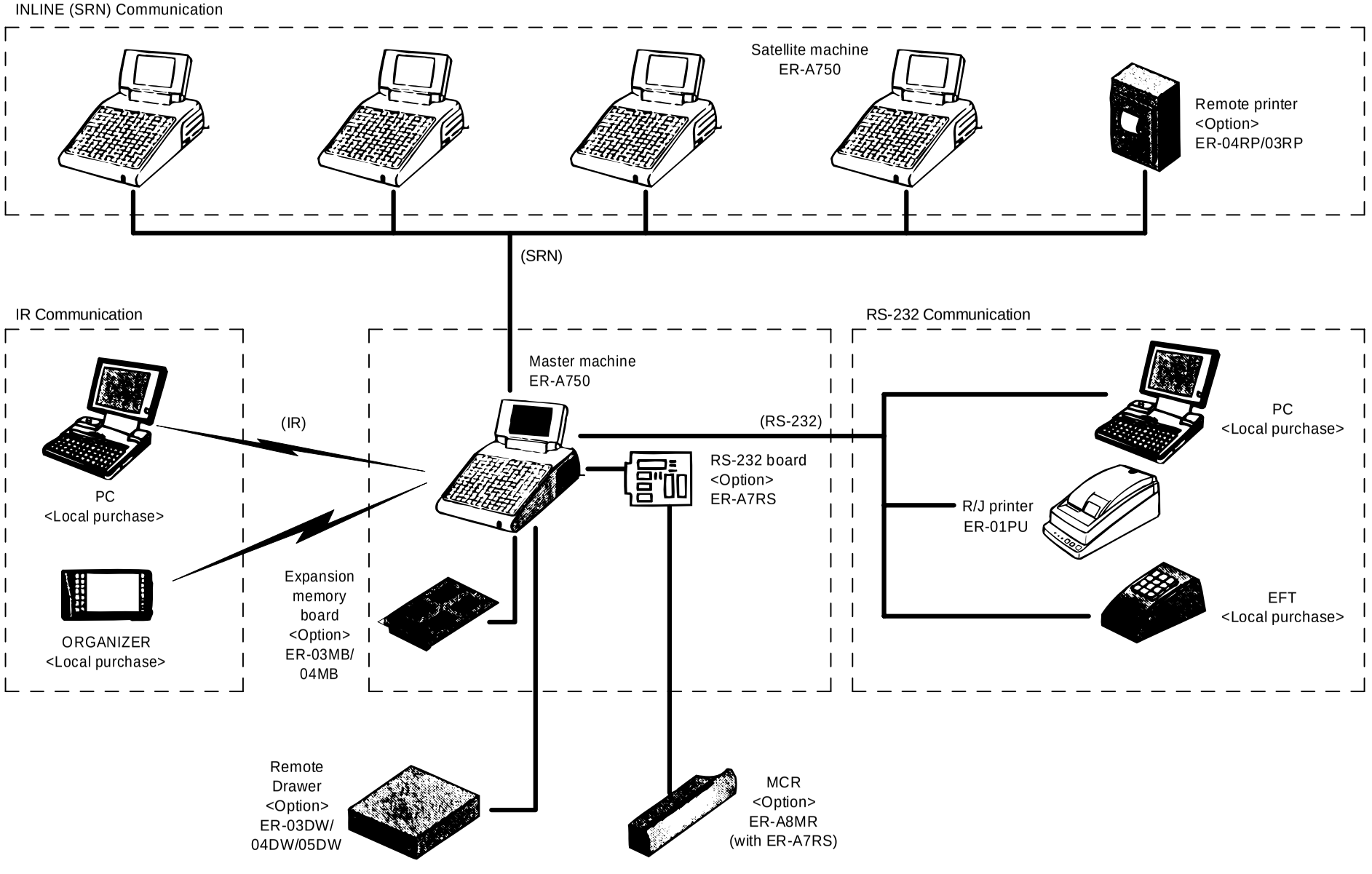
3) Display adjustment

You can adjust the brightness and contrast of the display by using the corresponding controls.


· Brightness control
Turning the control backwards darkens the display and turning it forwards brightens the display.
· Contrast control
Turning the control backwards darkens the display and turning it forwards lightens the display.

CHAPTER2. OPTIONS

1. System configuration



2. Options

No.	NAME	MODEL	DESCRIPTION
1	External printer	ER-01PU	via RS-232
2	Remote printer	ER-03RP	via SRN
		ER-04RP	
3	Slip printer	TM-295	via RS-232 Local purchase
		Indatec100	
4	Remote drawer	ER-03DW	Max. 2 units
		ER-04DW	
		ER-05DW	
5	Coin case	ER-48CC3	
		ER-48CC2	
		ER-58CC3	
6	Coin case cover	ER-01CV1 ~ 5	
		ER-02CV1 ~ 5	
		ER-03CV	
7	Expansion RAM board	ER-03MB	1 MB PS-RAM
		ER-04MB	2 MB PS-RAM
8	RS-232 I/F	ER-A7RS	RS-232 I/F: 2 ports MCR I/F
9	MCR (Magnet Card Reader)	ER-A8MR	via ER-A7RS
10	Data buck up system	ER-02FD	FD unit
		CE-IR2	Wireless I/F for IR communication
		CE-IR4	

3. Service tools

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	TERMINATOR	QCNCM7145RCZZ	AZ	For SRN in-line system
2	Expansion PWB	CKŌG−6724BHZZ	BQ	
3	MCR test card	UKŌG−6718RCZZ	BE	For ER-A8MR
4	RS-232 loop back connector	UKŌG−6705RCZZ	BC	For RS-232 connector
5	1 hole clerk key	LKGiM7377BH07	BA	Key No. 7
		LKGiM7377BH08	BA	Key No. 8
		LKGiM7377BH09	BA	Key No. 9
		LKGiM7377BH10	BA	Key No. 10
		LKGiM7377BH11	BA	Key No. 11
		LKGiM7377BH12	BA	Key No. 12
		LKGiM7377BH13	BA	Key No. 13
		LKGiM7377BH14	BA	Key No. 14
		LKGiM7377BH15	BA	Key No. 15
		LKGiM7377BH16	BA	Key No. 16
		LKGiM7377BH17	BA	Key No. 17
		LKGiM7377BH18	BA	Key No. 18
		LKGiM7377BH19	BA	Key No. 19
		LKGiM7377BH20	BA	Key No. 20
		LKGiM7377BH21	BA	Key No. 21
		LKGiM7377BH22	BA	Key No. 22
		LKGiM7377BH23	BA	Key No. 23
		LKGiM7377BH24	BA	Key No. 24
		LKGiM7377BH25	BA	Key No. 25
		LKGiM7377BH26	BA	Key No. 26
		LKGiM7377BH27	BA	Key No. 27
		LKGiM7377BH28	BA	Key No. 28
		LKGiM7377BH29	BA	Key No. 29

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
5	1 hole clerk key	LKGiM7377BH30	BA	Key No. 30
		LKGiM7377BH31	BA	Key No. 31
		LKGiM7377BH32	BA	Key No. 32
		LKGiM7377BH33	BA	Key No. 33
		LKGiM7377BH34	BA	Key No. 34
		LKGiM7377BH35	BA	Key No. 35
		LKGiM7377BH36	BA	Key No. 36
		LKGiM7377BH37	BA	Key No. 37
		LKGiM7377BH38	BA	Key No. 38
		LKGiM7377BH39	BA	Key No. 39
		LKGiM7377BH40	BA	Key No. 40
		LKGiM7377BH41	BA	Key No. 41
		LKGiM7377BH42	BA	Key No. 42
		LKGiM7377BH43	BA	Key No. 43
		LKGiM7377BH44	BA	Key No. 44
		LKGiM7377BH45	BA	Key No. 45
		LKGiM7377BH46	BA	Key No. 46
		LKGiM7377BH47	BA	Key No. 47
		LKGiM7377BH48	BA	Key No. 48
		LKGiM7377BH49	BA	Key No. 49
		LKGiM7377BH50	BA	Key No. 50
		LKGiM7377BH51	BA	Key No. 51
		LKGiM7377BH52	BA	Key No. 52
		LKGiM7377BH53	BA	Key No. 53
		LKGiM7377BH54	BA	Key No. 54
		LKGiM7377BH55	BA	Key No. 55
		LKGiM7377BH56	BA	Key No. 56
		LKGiM7377BH57	BA	Key No. 57
		LKGiM7377BH58	BA	Key No. 58
		LKGiM7377BH59	BA	Key No. 59
		LKGiM7377BH60	BA	Key No. 60
		LKGiM7377BH61	BA	Key No. 61
		LKGiM7377BH62	BA	Key No. 62
		LKGiM7377BH63	BA	Key No. 63
		LKGiM7377BH64	BA	Key No. 64
		LKGiM7377BH65	BA	Key No. 65
		LKGiM7377BH66	BA	Key No. 66
		LKGiM7377BH67	BA	Key No. 67
		LKGiM7377BH68	BA	Key No. 68
		LKGiM7377BH69	BA	Key No. 69
		LKGiM7377BH70	BA	Key No. 70
		LKGiM7377BH71	BA	Key No. 71
		LKGiM7377BH72	BA	Key No. 72
		LKGiM7377BH73	BA	Key No. 73
		LKGiM7377BH74	BA	Key No. 74
		LKGiM7377BH75	BA	Key No. 75
		LKGiM7377BH76	BA	Key No. 76
		LKGiM7377BH77	BA	Key No. 77
		LKGiM7377BH78	BA	Key No. 78
		LKGiM7377BH79	BA	Key No. 79
		LKGiM7377BH80	BA	Key No. 80
		LKGiM7377BH81	BA	Key No. 81
		LKGiM7377BH82	BA	Key No. 82
		LKGiM7377BH83	BA	Key No. 83
		LKGiM7377BH84	BA	Key No. 84
		LKGiM7377BH85	BA	Key No. 85

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
5	1 hole clerk key	LKGiM7377BH86	BA	Key No. 86
		LKGiM7377BH87	BA	Key No. 87
		LKGiM7377BH88	BA	Key No. 88
		LKGiM7377BH89	BA	Key No. 89
		LKGiM7377BH90	BA	Key No. 90
		LKGiM7377BH91	BA	Key No. 91
		LKGiM7377BH92	BA	Key No. 92
		LKGiM7377BH93	BA	Key No. 93
		LKGiM7377BH94	BA	Key No. 94
		LKGiM7377BH95	BA	Key No. 95
		LKGiM7377BH96	BA	Key No. 96
		LKGiM7377BH97	BA	Key No. 97
		LKGiM7377BH98	BA	Key No. 98
		LKGiM7377BH99	BA	Key No. 99
		LKGiM7377BH00	BA	Key No. 100
		LKGiM7377BHA1	BA	Key No. 101
		LKGiM7377BHA2	BA	Key No. 102
		LKGiM7377BHA3	BA	Key No. 103
		LKGiM7377BHA4	BA	Key No. 104
		LKGiM7377BHA5	BA	Key No. 105
		LKGiM7377BHA6	BA	Key No. 106
		LKGiM7377BHA7	BA	Key No. 107
		LKGiM7377BHA8	BA	Key No. 108
		LKGiM7377BHA9	BA	Key No. 109
		LKGiM7377BHA0	BA	Key No. 110
		LKGiM7377BHB1	BA	Key No. 111
		LKGiM7377BHB2	BA	Key No. 112
		LKGiM7377BHB3	BA	Key No. 113
		LKGiM7377BHB4	BA	Key No. 114
		LKGiM7377BHB5	BA	Key No. 115
		LKGiM7377BHB6	BA	Key No. 116
		LKGiM7377BHB7	BA	Key No. 117
		LKGiM7377BHB8	BA	Key No. 118
		LKGiM7377BHB9	BA	Key No. 119
		LKGiM7377BHB0	BA	Key No. 120
		LKGiM7377BHC1	BA	Key No. 121
		LKGiM7377BHC2	BA	Key No. 122
		LKGiM7377BHC3	BA	Key No. 123
		LKGiM7377BHC4	BA	Key No. 124
		LKGiM7377BHC5	BA	Key No. 125
		LKGiM7377BHC6	BA	Key No. 126

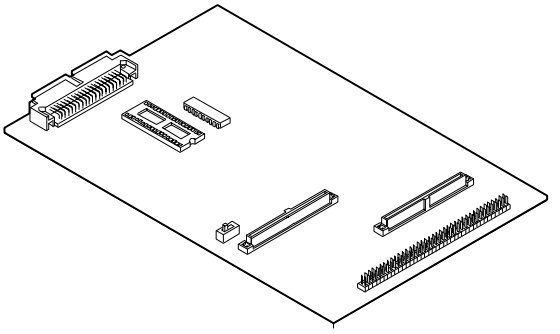
4. Supplies

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	STANDARD KEY SHEET	PSHEK6851BHZZ	AS	
2	PROGRAMMING KEY SHEET	PSHEK6852BHZZ	AH	
3	BLANK KEY SHEET	PSHEK6818BHZZ	AQ	

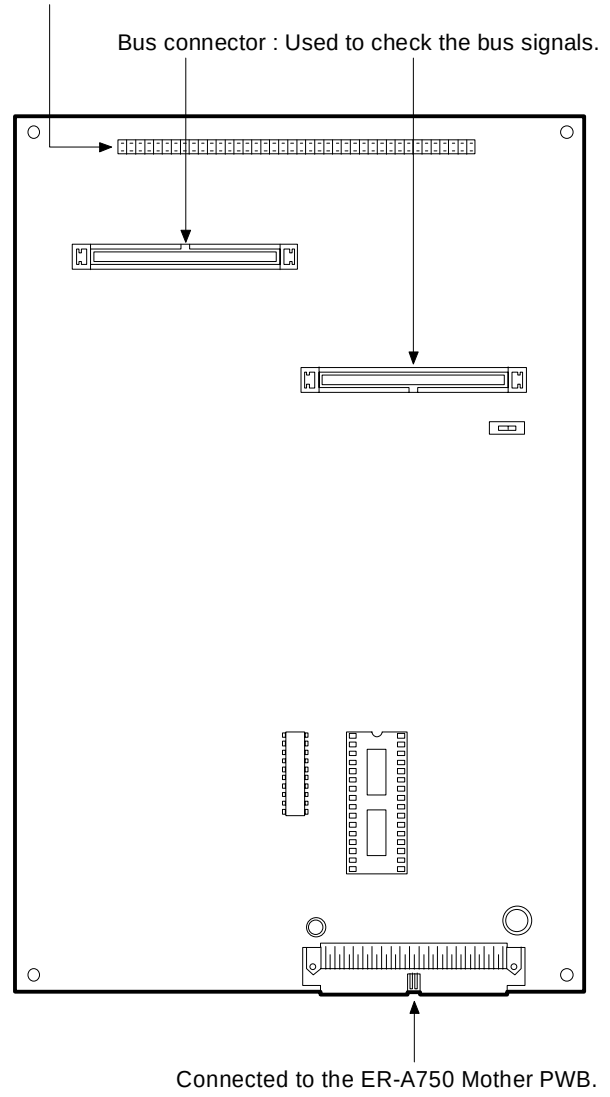
5. How to use service tools

5-1. Expansion PWB : CKOG-6724BHZZ

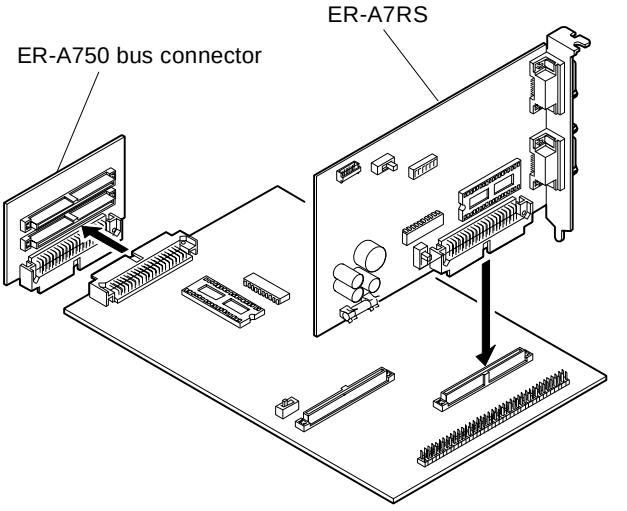
- Extrenal view



- Plain view

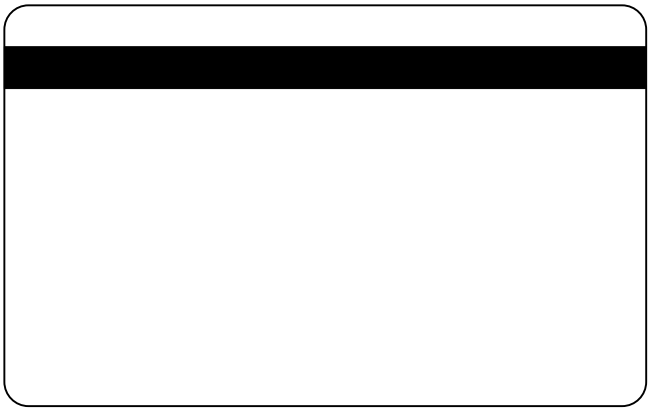


- Connection diagram



5-2. MCR test card: UKOG-6718RCZZ

- Used when executing the diagnostics of the ER-A8MR.
- External view



CHAPTER 3. SERVICE PRECAUTION

1. Adjustment for SRN (IN-LINE) interface circuit

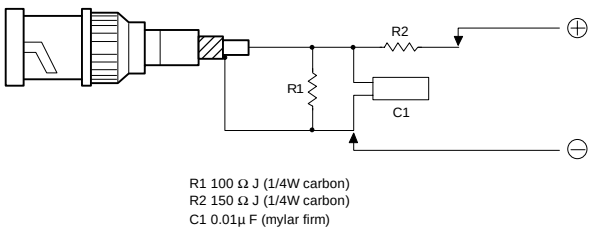
If transistor Q10 in the transmitter/receiver section has been replaced or if the SRN level requires readjustment, the following alignment is required:

1) Tools and Instruments Required

① Oscilloscope (50MHz or better). 1

② ER-A750 1

2) Dummy Network Specifications



R1 100 Ω J (1/4W carbon)
R2 150 Ω J (1/4W carbon)
C1 0.01μ F (mylar firm)

Fig. 1 Dummy network

The oscillator should be connected to the points indicated by ⊕ and ⊖.
⊕: Connect the positive side of the oscillator.
⊖: Connect the negative side of the oscillator.

3) Connections

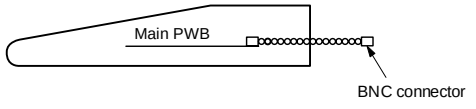


Fig. 2

Attach the BNC connector to the SRN connector (CON 15) on the main PWB.

4) Alignment Procedure

① When Using an Oscillator

a) Checking the 1MHz oscillator output

Using an oscilloscope check the 1MHz oscillator's output waveform.

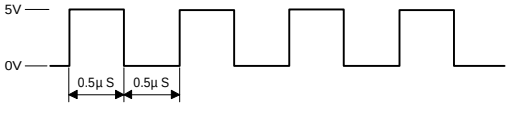


Fig. 3 1MHz oscillator output waveform

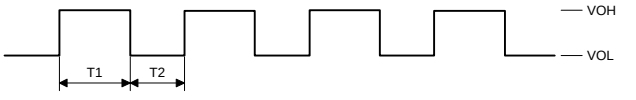
NOTE: The oscillator used should have an output impedance of 50Ω.

b) Connecting the oscillator and its adjustment

Connect a dummy network or branch-trunk network to the output of the SRN connector (CON 15), and connect the oscillator to the dummy or branch-trunk network.

∗ Waveform adjustment

Adjust VR4 until the signal waveform as shown in Fig. 5 is obtained across IC34 (pin 1 of the 75115) and GND pin.
Turning VR4 clockwise extends the interval of T1.



T1 = 580 to 620ms
T2 = 380 to 420ms

Fig. 5 Receiver regeneration waveform (with dummy network)

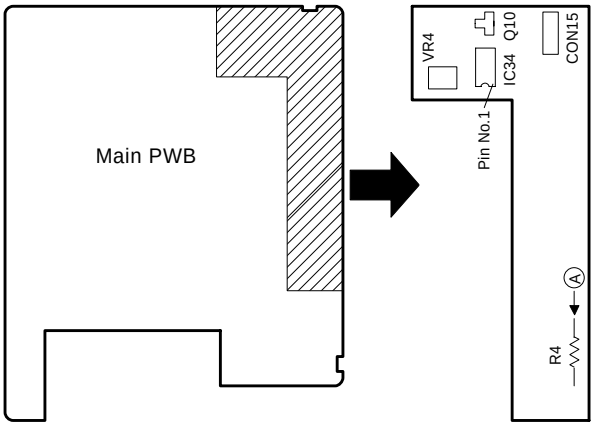


Fig. 6 Board location

② When the Branch Trunk Network and Two POS'S are Available.

a) Connecting terminals

Both ends of the network must be terminated with a 50Ω terminator. If only two active terminals are tested and left on the network, disconnect all other terminals from the network. (In this case as well, both ends of the trunk network must be terminated with 50Ω).

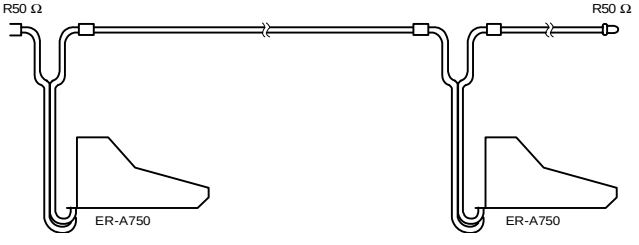


Fig. 7 Terminal connection

b) Receive level adjustment

i) Turn on both the receiver terminal and the transmitter terminal.

ii) Run the diagnostic program "Flag send check" on the transmitter terminal to send a flag.

iii) Checking transmitter terminals' output waveform
Using an oscilloscope, check the transmitter terminal's output signal waveform.

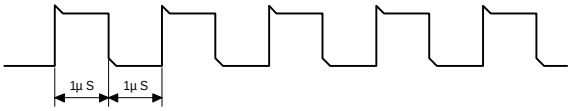


Fig. 8 Transmitter terminal's output waveform (at transmitter output)

At the receiver terminal, the transmitter terminal's output waveform is subject to attenuation and distortion due to the length of the trunk cable (this depends on the characteristics of the cable itself).

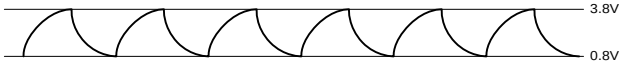


Fig. 9 Example of distorted signal waveform at the receiver terminal (RG58/U 400m)

Adjust the receiver terminal adjust VR4 (20kΩ) on the main PWB until the waveform as shown in Fig. 10 is obtained at IC34 (pin 1 of the 75115). (For the location of VR4, see Fig. 6 Board location of this subsection).
Clockwise rotation of VR4 extends the High level pulse width of the signal at IC34 (pin 1 of the 75115).

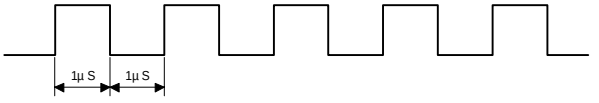


Fig. 10 Waveform at IC34 (pin 1 of the 75115 IC in the receiver terminal)

5) Other Checks (These Checks should be done After the Receive Level Adjustment is Completed).

① Line driver bias control circuit

Make sure that the voltage at the Ⓐ-side lead of the R4 resistor (150Ω, 3W) shown in Fig. 6 is properly switched.

Procedure:

i) Connect a terminating resistor or read network to the BNC connector, QCNW-6856RCZZ (Fig. 2).

ii) Run the diagnostic program "Data send check", and make sure that the voltage at point Ⓐ (in Fig. 6) is switched as shown in Fig. 11.

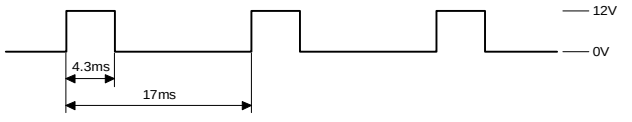


Fig. 11 bias circuit switching waveform

iii) If the waveform as shown in Fig. 11 is not obtained, it is most probable that transistor Q10 (2SC4699) is defective.

② For the other check items, refer to DIAGNOSTICS SPECIFICATIONS

2. Battery label

The battery label is attached to the main chassis on the back surface of the set.
The battery label has the column to show the battery replacement date. Put down the date in the following cases:
(The battery life is about 3 years after replacement.)

- When the set is installed.
- When the battery is replaced after installation.

CAUTION: When the time written below comes, ask your dealer for a replacement of the battery.
VORSICHT: Wenn die untenbenannte Zeit erreicht wird, ersuchen Sie bitte Ihren Fachhändler um den Austausch der Batterie.
PRECAUTION: Lorsque le temps écrit ci-après arrive, demander à votre revendeur local de remplacer la batterie par une nouvelle.
ADVERTENCIA: Cuando se alcance el tiempo indicado abajo, solicite a su distribuidor que reemplace la batería.
Time to replace : _____ Austauschzeit : _____ Le temps de la remplacer : _____ Tiempo de reemplazo : _____

3. Precautions in installing optional RAM PWBs

1) Background

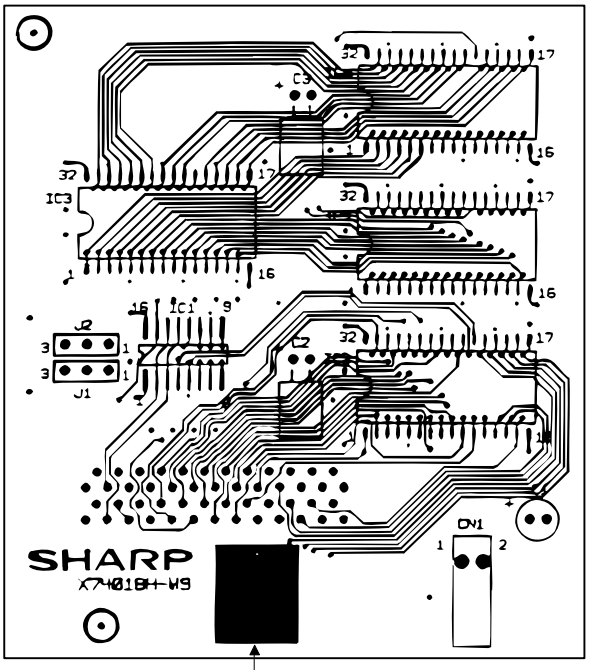
The ER-A750 can use the ER-03MB or the ER-04MB as an optional RAM PWB. The ER-03MB and the ER-04MB are available in two versions according to the difference in access time of the pseudo-SRAM.

(1) 150 ns access time version (Not marked with "○"; manufactured before June, 1996; shipped only to North America and Europe)

(2) 120 ns access time version (Marked with "○"); manufactured after July, 1996 These two versions can be identified, one from the other, by whether or not the "○" mark is stamped on the white background as shown in Fig. 1 and by the marking on the case. (See Fig. 1.)

PWB marking

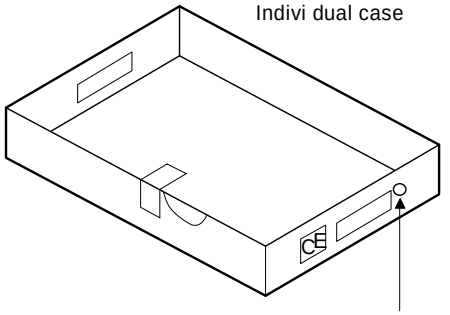
(ER-03MB/04MB PWB Face side)



Imprint "○" on this white area.

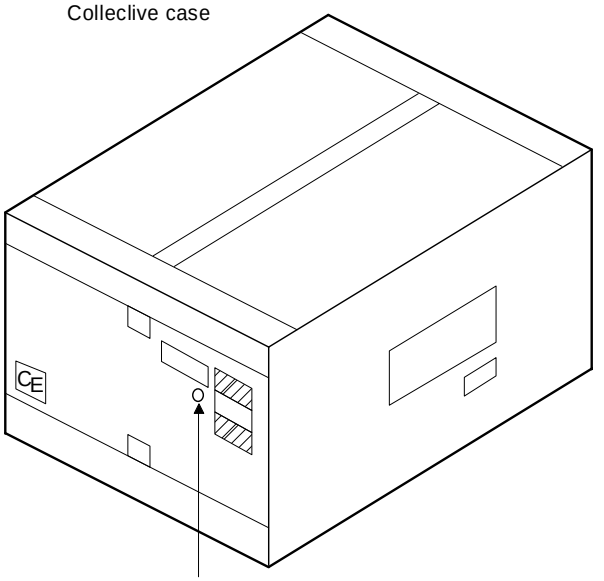
Packing case

Indivi dual case



Imprint "○" on the right side of the model rabel.

Colleclive case



Imprint "○" under the model label.

2) Cautions to be exercised when using the RAM PWBs with the ER-A750

When using the above-mentioned RAM PWB version (1) with the ER-A750, it is necessary to correct the RAM access timing. Use of the above-mentioned RAM PWB version (2) does not require the correction of the RAM access timing. For this purpose, a hardware jumper (JP1), designed to judge to determine whether or not to correct the RAM access timing, is located on the main PWB of the ER-A750 (Fig. 2). Before installing an optional RAM PWB, check its version by referring to the description given in the above-mentioned (1) and (2) and set the jumper as shown below. (The ER-A750 has been factory-set for 150ns access time and TP cycle inserted.)

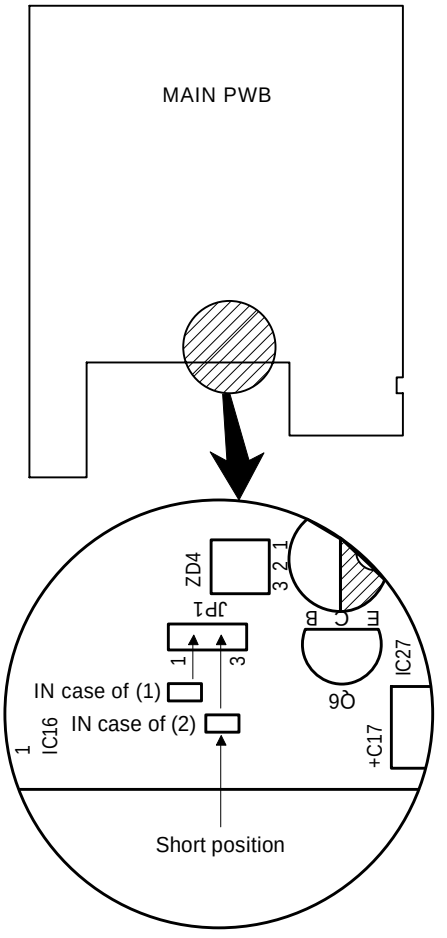
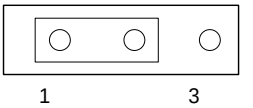
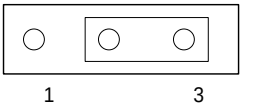


Fig. 3 Setting of the JP1 on the main PWB of the ER-A750

(1) Setting when the ER-03MB or the ER-04MB is not marked with "○"
(Position to which the ER-A750 has been factory-set)



(2) Setting when the ER-03MB or the ER-04MB is marked with "○"



3) Difference in operation according to the setting of the jumper

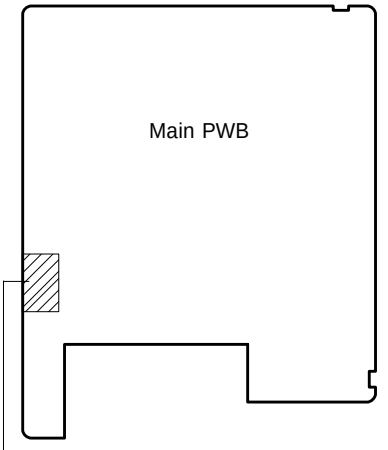
Only when the ER-03MB or the ER-04MB is used in the above setting state (1) will one cycle (i.e., cycle for generating pre-charge time of the quasi-SRAM: TP cycle) of access be additionally inserted into the CPU, thereby delaying the CPU speed slightly.

4) Factory-setting of the ER-A750

The ER-A750 has been factory-set so that the JP1 is in the setting state (1) (TP cycle inserted). However, if it has neither the ER-03MB or the ER-04MB installed to it, this is automatically detected by software, so the additional insertion of the TP cycle is not performed.

Note:
When installing the ER-03MB or the ER-04MB, check the position of the jumper by referring to Fig. 3.
Improper setting of the jumper may result in malfunction.

4. IR module (PRM-850) soldering conditions



When replacing the IR module (IC1), observe the following conditions.

Solder the IR module with the solder tip temperature at 280 degrees C within 3 sec.

5. IPL (Initial Program Loading) function

1) Introduction

The application software of the ER-A750 is written in the flash ROM (IC6: VHILH80S01-1). In the following cases, writing procedure of the application software into the flash ROM is required:

- When the flash ROM (IC6: VHILH80S01-1) is replaced with new one. The service part flash ROM does not include the application software in it.
- When IPL writing is required because of change in the application software.

∗ The service part of the main PWB unit (CPWBX7510BH01) includes the flash ROM (IC6: VHILH80S01-1) with the application software written in it, and there is no need for writing the application software when replacing the main PWB unit.

2) IPL procedure

There are two ways of IPL procedures.

- IPL from P-ROM via ER-A7RS
- IPL from PC via IR (infrared) communication

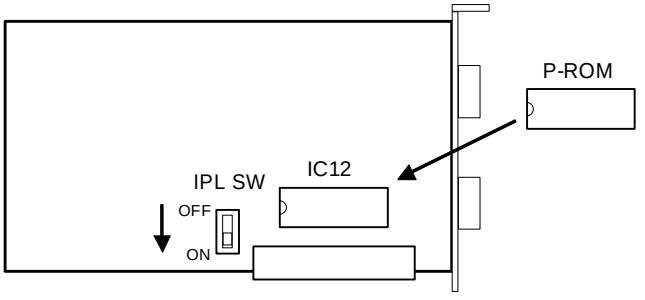
The detailed descriptions on the above procedures are given below.

3) IPL from P-ROM via ER-A7RS

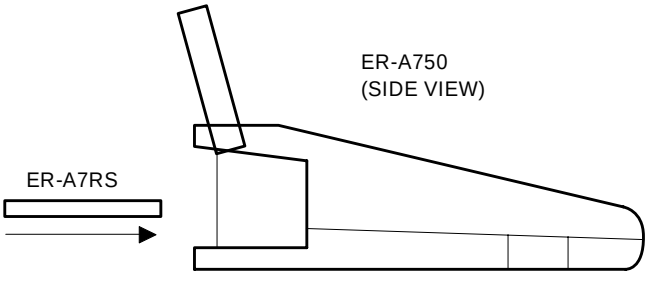
(1) Install the master ROM to the IC socket (IC12) on the ER-A7RS.

Master ROM: Part code: VHI27801RAB1A

(2) IPL switch on the ER-A7RS: Set the IPL SW to ON position.



(3) Install the ER-A7RS to the ER-A750. (The ER-A750 power should be turned OFF.)



(4) Turn on the power of the ER-A750.

(5) The following display is shown and the IPL procedure is started.

When the procedure is completed, the message of "Completed." is shown.

LCD DISPLAY

```
IPL from PROM
C0 C1 C2 C3 C4 C5 C6 C7
C8 C9 CA CB CC CD CE CF
Completed.
```

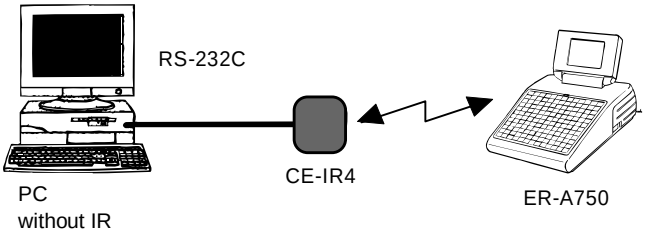
(6) Turn off the power of the ER-A750.

(7) Remove the ER-A7RS from the ER-A750.

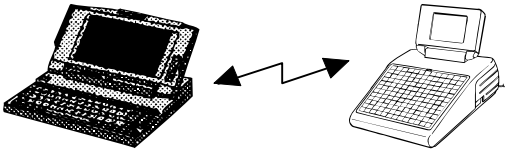
(8) Perform the master reset. (Refer to CHAPTER 4.)

4) IPL from PC via IR (infrared) communication

(1) IR communication between the ER-A750 and PC is as follows:

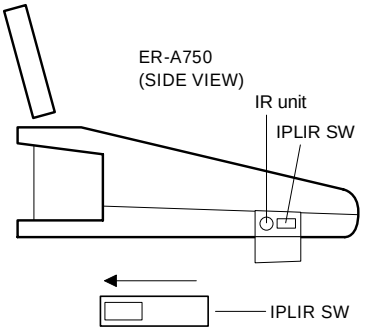


1. PC+CE-IR4 system



2. PC only system

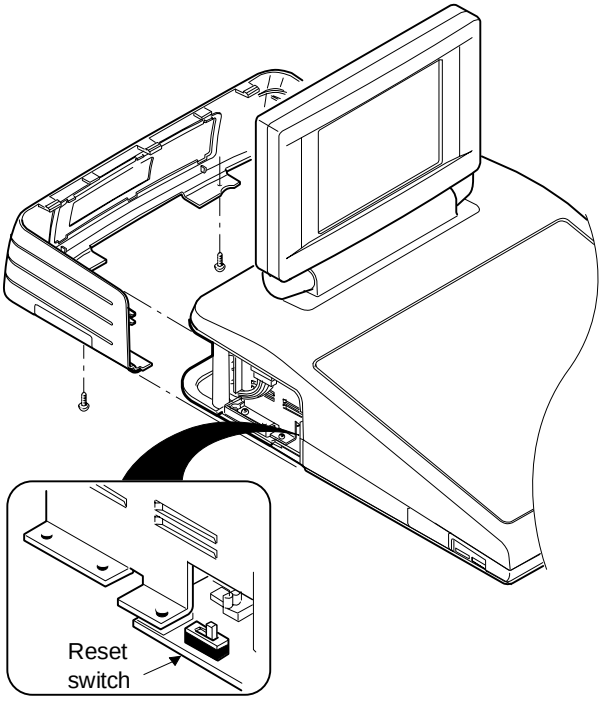
(2) Procedures on the PC side and on the ER-A750 side are as follows:

No	Procedure on P.C. side	No	Procedure on ER-A750 side
1	Copy “A7IPL.EXE” and S-type ROM object file (ex. “A750_0A.ROM) into your Personal Computer (P.C.). ∗ “A7IPL.EXE” and S-type ROM object file is separately supplied.		
		2	Turn OFF the power.
		3	Select IPL Receiving Mode. Set IPL switch “ON”. ① Open the IR cover of the ER-A750. ② IPL switch: Set the IPLIR SW to the left side when viewed from the front. 
		4	Turn ON the power.
		5	Starting of IPL Receiving Mode. ER-A750 shows “IPL from IR” IPL from IR
6	Connect P.C. and ER-A750 via IR.		

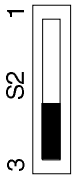
7	Execute “A7IPL.EXE” on P.C. Operation: >A7IPL A750_0A.ROM (“A750_0A.ROM” is file name of S-type ROM object.)		
8	Program data is sent to ER-A750 automatically.	8	Program data is received from P.C. automatically. IPL from IR Connected IRDA 115200 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF
9	“A7IPL.EXE” is completed. P.C. shows “Completed.”	9	ER-A750 shows “Completed.” IPL from IR Connected IRDA 115200 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF Completed.
		10	Turn OFF the power.
		11	Select Normal Mode. Set IPL switch “OFF”.
		12	Execute “Master reset” on ER-A750.
			End

CHAPTER 4. SRV RESET (Program Loop Reset) and switch to SRV mode

In the ER-A750, the following reset switch (location No.: S2) is used to switch to the service (SRV) mode and to reset.



1Side(Rear side):"ON" position(Reset state)



3Side(Front side):"OFF" position(Reset cancel)

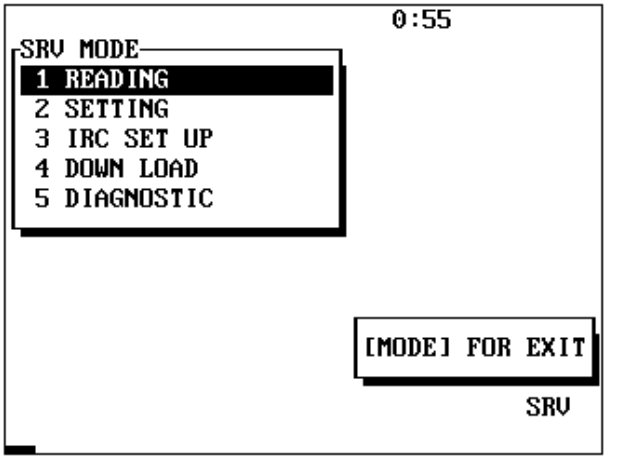
SRV. reset

Used to return the machine back to its operation state after a lock up has occurred.

PROCEDURE

1) Turn off the AC switch.
2) Set the reset switch to “OFF” position
3) Turn on the AC switch.
4) Turn to “ON” the reset switch.
5) The SRV mode is displayed as shown below.

   DISPLAY:



CHAPTER 5. MASTER RESET (All Memory Clear)

There are two possible methods to perform a master reset.

MRS-1 (Master resetting 1)

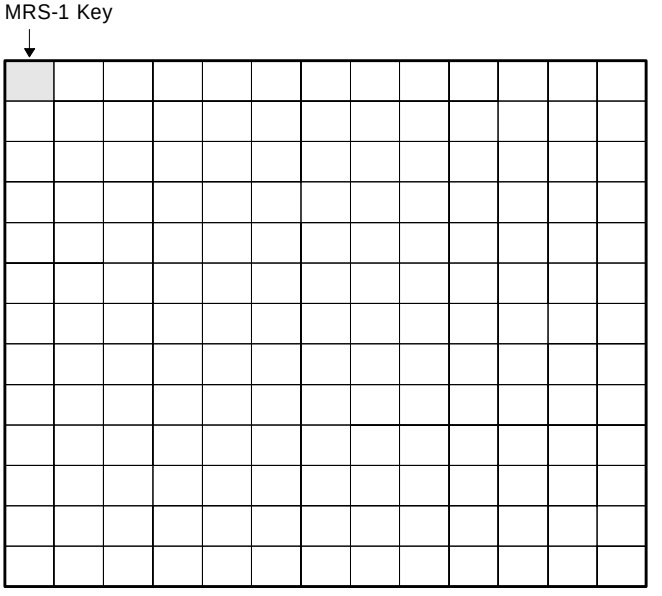
Used to clear all memory contents and return machine back to its initial settings.

Return keyboard back to default for default kyeboard layout.

PROCEDURE

1) Turn off the AC switch.
2) Set the reset switch to “OFF” position
3) Turn on the AC switch.
4) While holding down MRS-1 key , turn to “ON” the reset switch.

   ∗ MRS-1 key : The key located on Left upper corner of the key-board.



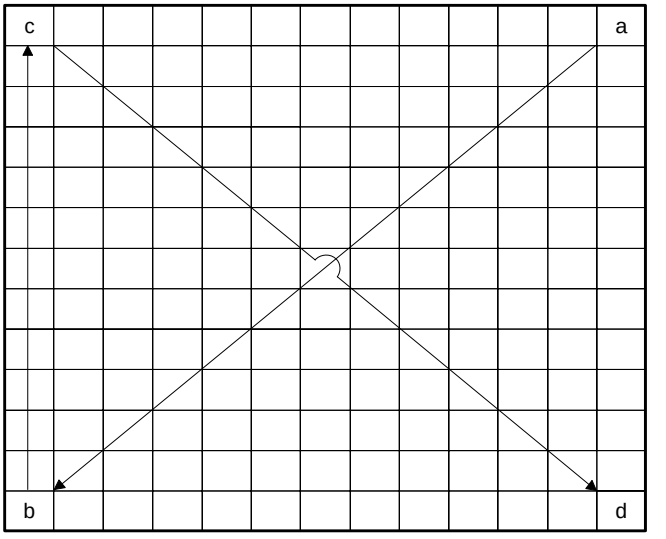
Keyboard layout

5) Enter the password key operation

   DISPLAY:

   ENTER PASSWORD

   Password input procedure: Press the four corners of the key-board in the sequence of a, b, c, and d.



Keyboard layout

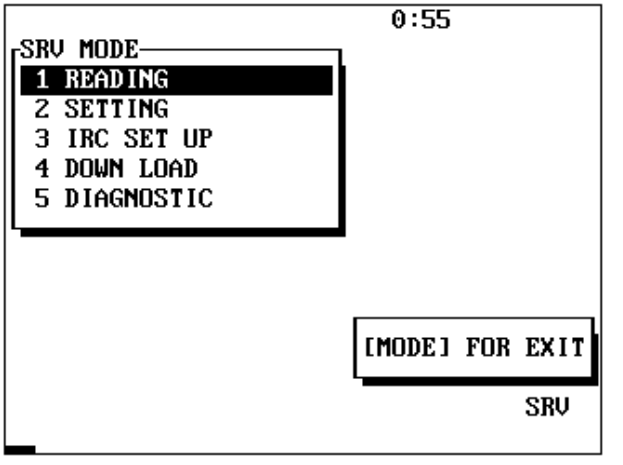
6) Master reset is started.

   DISPLAY:

   MASTER RESET

7) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

   DISPLAY:



MRS-2 (Master resetting 2)

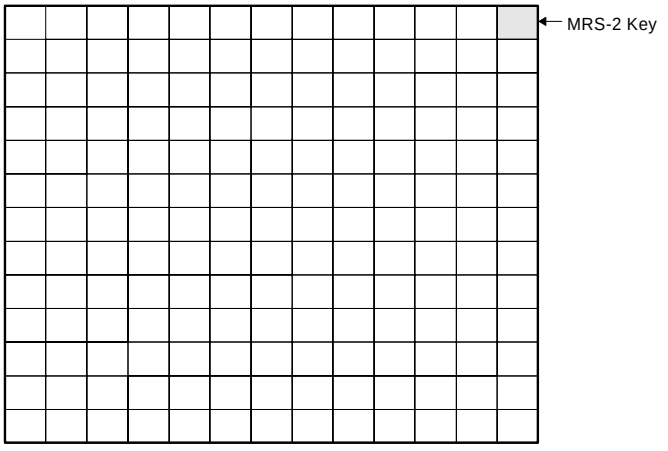
Used to clear all memory and keyboard contents. This reset returns all programming back to defaults.

The keyboard must be entered by hand. This reset is used if an application needs different keyboard layout other than that supplied by a normal MRS-1.

PROCEDURE

1) Turn off the AC switch.
2) Set the reset switch to “OFF” position
3) Turn on the AC switch.
4) While holding down MRS-2 key , turn to “ON” the reset switch.

   ∗ MRS-2 key : The key located on Right upper corner of the keyboard.



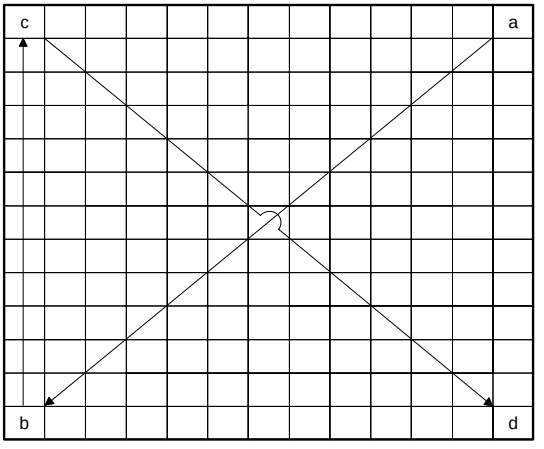
Keyboard layout

5) Enter the password key operation

   DISPLAY:

ENTER PASSWORD

   Password input procedure: Press the four corners of the key-board in the sequence of a, b, c, and d.



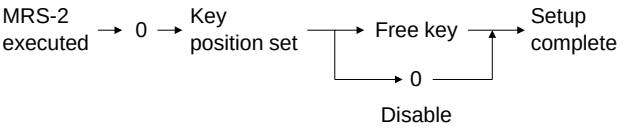
Keyboard layout

6) Set the fixed keys in the table below. (Start from the zero “0” key, The keys are displayed sequentially.)

   DISPLAY:

ENTER 0 KEY

   [Key setup procedure]



   NOTES:

   ∗1: When the 0 key is pressed, the key of the key number on display is disabled.

   ∗2: Push the key on the position to be assigned. With this, the key of the key number on display is assigned to that key position.

   ∗3: When relocating the keyboard, the PGM 1/2 mode use standard key layout.

Key No.	Key name	Key No.	Key name	Key No.	Key name
001	“0” key	011	“00” key	021	RIGHT “→” key
002	“1” key	012	“000” key	022	“CANCEL” key
003	“2” key	013	Decimal point “•” key	023	“ENTER” key
004	“3” key	014	“CL” key	024	“TL” key
005	“4” key	015	“⊗” key		
006	“5” key	016	“SBTL” key		
007	“6” key	017	“MODE” key		
008	“7” key	018	UP “↑” key		
009	“8” key	019	DOWN “↓” key		
010	“9” key	020	LEFT “←” key		

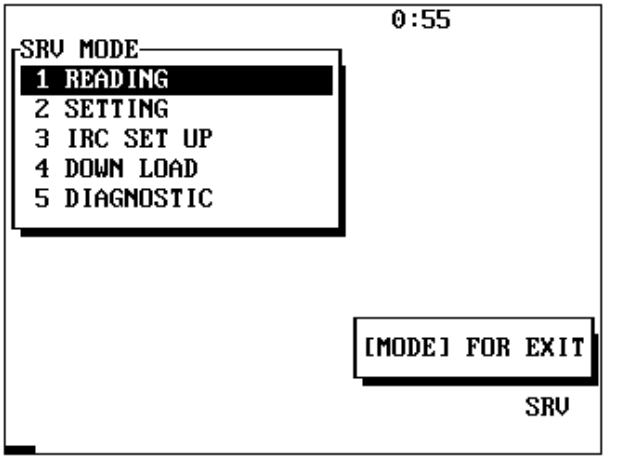
7) Master reset is started.

   DISPLAY:

MASTER RESET

8) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

   DISPLAY:



CHAPTER 6. DIAGNOSTICS SPECIFICATIONS

CONTENTS

1. General 1
2. System configuration 1
   2-1. Test system 1
3. Diagnostics 1
   1) Master reset procedure 1
   2) Program reset (service reset) procedure 1
   3-1. Execution of diagnostics 1
   3-2. RAM Diagnostics 2
   1) Standard RAM Check 2
   2) VRAM Check 2
   3) ER-03MB Check 3
   4) ER-04MB Check 3
   3-3. ROM & SSP Diagnostics 4
   1) Standard ROM Check 4
   2) SERVICE ROM Check 4
   3) SSP Check 4
   3-4. Timer & Keyboard & Clerk Switch Diagnostics 5
   1) Timer Check 5
   2) Keyboard Check 5
   3) Clerk SW Check 5
   3-5. RS232 I/F Diagnostics 5
   1) CHANNEL Check 5
   2) CH1 Check 6
   3) CH2 Check 6
   4) CH3 Check 6
   5) CH4 Check 6
   6) CH5 Check 6
   7) CH6 Check 6
   8) CH7 Check 6
   3-6. Liquid Crystal Display Diagnostics 7
   1) Liquid Crystal Display Check 7
   3-7. Rear Display Diagnostics 7
   1) Rear Display Check 7
   3-8. SHARP Retail Network Diagnostics 8
   1) SRN Self Check 8
   2) SRN Flag Send Check 9
   3) SRN Data Send Check 9
   4) Data Transmission Check 9
   3-9. IrDA & ASK Diagnostics 10
   1) IrDA & ASK Check 10
   2) IrDA & ASK Check (checker mode) 10
   3) Data Transmission Check (Receive mode) 10
   4) Data Transmission Check (Send mode) 11
   3-10. Magnetic Card Reader Diagnostics 11
   1) Magnetic Card Reader Check 11
   3-11. Drawer Diagnostics 11
   1) Drawer 1 Check 11
   2) Drawer 2 Check 11

1. General

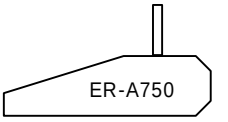
This diagnostics program is used for simplified check of the ER-A750 series operations in servicing.

The diagnostics program is built in the standard ROM.

2. System configuration

2-1. Test system

ER-A750 only



3. Diagnostics

Starting the diagnostics

This diagnostics program is written in the external ROM and executed by the CPU (H8/510). To operate this program, the following conditions must be satisfied.

① The power for the logic system is proper.
(+5V, VRAM, VCKDC, POFF, +24V)

② The input/output pins and the internal logic of the CPU are normal. In addition, CKDC7, MPCA7, the system bus, and the standard ROM/RAM are normal.

To start the machine for the first time, perform the master reset.

In order to add an option unit when the machine is normally operating, perform the program reset.

1) Master reset procedure

① Turn off the power.

② Set the CKDC reset switch to RESET position.

③ Turn on the power.

④ While pressing the specified key, set the CKDC reset switch to the normal position.

2) Program reset (service reset) procedure

① Turn off the power.

② Set the CKDC reset switch to RESET position.

③ Turn on the power.

④ Set the CKDC reset switch to the normal position. (Do not press any key.)

3-1. Execution of diagnostics

To start the diagnostics, select "DIAGNOSTICS" with the cursor in the menu selection in SRV mode, and press the enter key.

The DIAG MAIN MENU is started and the following menu screen is display. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the individual diagnostics program is completed, the display returns to the menu screen. To terminate the diagnostics, press the CANCEL key. Then the display returns to the SRV mode menu screen.

```
ER-A750 Diagnostics  V 1.0A

   Product & Test Diagnostics
   RAM Diagnostics
   ROM & SSP Diagnostics
   Clock & Keyboard & Clerk Diagnostics
   Serial I/O Diagnostics
   LCD Diagnostics
   Rear Display Diagnostics
   SRN Diagnostics
   IrDA Diagnostics
   MCR Diagnostics
   Drawer Diagnostics
   Diagnostics End
```

"Product & Test Diagnostics" is used only in the production process, and must be not used in servicing.

3-2. RAM Diagnostics

This diagnostics is used to test the standard RAM and the expansion RAM.

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed.

```
RAM Diagnostics

   Standard RAM Check
   VRAM Check
   ER-03MB Check
   ER-04MB Check
```

1) Standard RAM Check

① Check content

For the pseudo SRAM of the standard RAM 512KB, the following check is performed. The memory contents will not be changed by this check.

The following processes are performed for the memory address (180000H ~ 1FFFFFH) to be checked.

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated.

Check point address = 180000H, 180001H
180002H, 180004H
180008H, 180010H
180020H, 180040H
180080H, 180100H
180200H, 180400H
180800H, 181000H
188000H, 190000H
1A0000H, 1C0000H

② Display

```
Standard RAM Check

  Standard memory size : 512KB PASS!!(or ERROR!!)

  Error Address  xxxxxxH
      Write Data  xxxxH
       Read Data  xxxxH
```

The error address and the bit are displayed only when the error occurs. (If the error does not occur, they are not displayed.)

③ Terminating procedure

After completion of check, press the CANCEL key.

2) VRAM Check

① Check content

The following check on VRAM is executed. The memory contents will not be changed by the check.

The following processes are performed for the check address (100000H ~ 107FFFH).

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed in the above check sequence.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated.

Check point address = 100000H, 100001H
100002H, 100004H
100008H, 100010H
100020H, 100040H
100080H, 100100H
100200H, 100400H
100800H, 101000H
102000H

② Display

```
VRAM Check

   VRAM memory size : 32KB    PASS!!(or ERROR!!)

   Error Address  xxxxxxH
       Write Data  xxxxH
        Read Data  xxxxH
```

The error address and the bit are displayed only when the error occurs. (If the error does not occur, they are not displayed.)

③ Terminating procedure

After completion of check, press the CANCEL key.

3) ER-03MB Check

① Check content

The ER-03MB presence check is performed in the following procedure. The memory contents will not be changed by this check.

- 55AAH is written into 2FFFFEH.
- 2FFFFEH is read and compared with 55AAH. If the both data are correct, the following procedure is performed. If not, "Extended RAM size: 0KB" is displayed and the check is terminated.
- 55AAH is written into 3FFFFEH.
- 3FFFFEH is read and compared with 55AAH. If the both data are not correct, the following procedure is performed. If correct, "Extend RAM is : ER-04MB" is displayed and the check is terminated.

For the ER-03MB, the following check is performed.

The following processes are performed for the check address (200000H ~ 2FFFFFH).

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed in the above check sequence.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated.

Check point address = 200000H, 200001H
200002H, 200004H
200008H, 200010H
200020H, 200040H
200080H, 200100H
200200H, 200400H
200800H, 201000H
202000H, 204000H
208000H, 210000H
220000H, 240000H
280000H

② Display

```
ER-03MB Check

   Extended RAM size : 1024KB  PASS!!(or ERROR!!)

   Error Address  xxxxxxH
       Write Data  xxxxH
        Read Data  xxxxH
```

The error address and the bit are displayed only when the error occurs. (If the error does not occur, they are not displayed.)

③ Terminating procedure

After completion of check, press the CANCEL key.

4) ER-04MB Check

① Check content

The ER-04MB presence check is performed in the following procedure. The memory contents must not be changed by this check.

- 55AAH is written into 3FFFFEH.
- 3FFFFEH is read and compared with 55AAH. If the both data are correct, the following procedure is performed. If not, go to ????????.
- 55AAH is written into 2FFFFEH.
- 2FFFFEH is read and compared with 55AAH. If the both data are correct, "Extend RAM is : ER-03MB" is displayed and the check is terminated. If not, "Extended RAM size : 0KB" is displayed and the check is terminated.

For the ER-04MB, the following check is performed.

The following processes are performed for the check address (200000H ~ 3FFFFFH).

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed in the above check sequence.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated without performing the check.

Check point address = 200000H, 200001H
200002H, 200004H
200008H, 200010H
200020H, 200040H
200080H, 200100H
200200H, 200400H
200800H, 201000H
202000H, 204000H
208000H, 210000H
220000H, 240000H
280000H, 300000H

② Display

```
ER-04MB Check

   Extended RAM size : 2048KB  PASS!!(or ERROR!!)

   Error Address  xxxxxxH
       Write Data  xxxxH
        Read Data  xxxxH
```

The error address and the bit are displayed only when the error occurs. (If the error does not occur, they are not displayed.)

③ Terminating procedure

After completion of check, press the CANCEL key.

3-3. ROM & SSP Diagnostics

The standard ROM and the service ROM are checked. The SSP circuit is also checked.

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed.

```
ROM & SSP Check

   Standard ROM Check
   Service ROM Check
   SSP Check
```

1) Standard ROM Check

① Check contents

The standard ROM area (C00000H ~ CFFFFFH) is added in the unit of byte. If the lower two digits of the result is 10H, it is normal. The ROM version and the model name code which are stored in address CFFFE0H ~ CFFFEFH where the ROM version and the check sum correction data are stored are displayed. The format of data (ASCII) to be stored is as follows:

CFFFE0H ~ CFFFEFH: Model name code (example: ER-A750. Display is made up to 00H of data.)

CFFFF0H ~ CFFFF9H: 27801R****(****=PROGRAM VERSION)

CFFFFAH ~ CFFFFBH: BLOCK NO. ("CO" ~ "CF")

CFFFFCH: TERMINATOR ("=")

CFFFFDH ~ CFFFFEH: BLOCK VERSION (example "00")

CFFFFFH: CHECK SUM CORRECTION DATA

The flash ROM used as the standard ROM has rewriting block of 64KB as the unit. To control the version in each block, the composition is the same as the above CFFFF0H or later and arranged in each 64KByte. At that time, correction is made so that the sum of each block becomes 01H, and the total of 1MByte is 10H.

The program version of the IPL is displayed so that 0PAGE where the IPL is stored is individually controlled.

② Display

```
Standard ROM Sum Check      : PASS!!(or ERROR!!)
IPL PROGRAM Version
                **
APL PROGRAM Version              ← Displays the version.
        27801R****  ERA750
BLOCK Version
              C0=**,C1=**,C2=**,C3=**
              C4=**,C5=**,C6=**,C7=**
                   :
```

③ Terminating procedure

After displaying the check result, press the CANCEL key to terminate the check.

2) SERVICE ROM Check

① Check content

The standard ROM area (D00000H ~ DFFFFFH) is added in the unit of byte. If the lower two digits of the result is 10H, it is normal. The ROM version and the model name code which are stored in address DFFFE0H ~ DFFFEFH where the ROM version and the check sum correction data are stored are displayed. The format of data (ASCII) to be stored is as follows:

DFFFE0H ~ DFFFEFH: Model name code (example: ER-A750. Display is made up to 00H of data.)

DFFFF0H ~ DFFFF9H: 27801R****(****=PROGRAM VERSION)

DFFFFAH ~ DFFFFBH: BLOCK NO. ("CO" ~ "CF")

DFFFFCH: TERMINATOR ("=")

DFFFFDH ~ DFFFFEH: BLOCK VERSION (example "00")

DFFFFFH: CHECK SUM CORRECTION DATA

This SERVICE ROM allows to write into the FLASH ROM when re-execution is impossible because of an abnormality during rewriting into the FLASH ROM. The composition is the same as the standard ROM.

The program version of the IPL is displayed so that 0PAGE where the IPL is stored is individually controlled.

② Display

```
Service ROM Sum Check    : PASS!!(or ERROR!!)
IPL PROGRAM Version
                **
APL PROGRAM Version              ← Displays the version.
        27801R****  ERA750
BLOCK Version
              C0=**,C1=**,C2=**,C3=**
              C4=**,C5=**,C6=**,C7=**
                   :
```

③ Terminating procedure

After displaying the check result, press the CANCEL key to terminate the check.

3) SSP Check

① Check content

By starting this check program, the SSP setting for checking is automatically performed and the SSP check is executed and the result is displayed.

The SSP check sets data for check in the vacant space in the SSP entry register, and deletes the data for check after completion of checking. Therefore, the already set data are not changed by this check.

② Display

```
SSP Check

   SSP (NMI) Check          : PASS!!(ERROR!!)
```

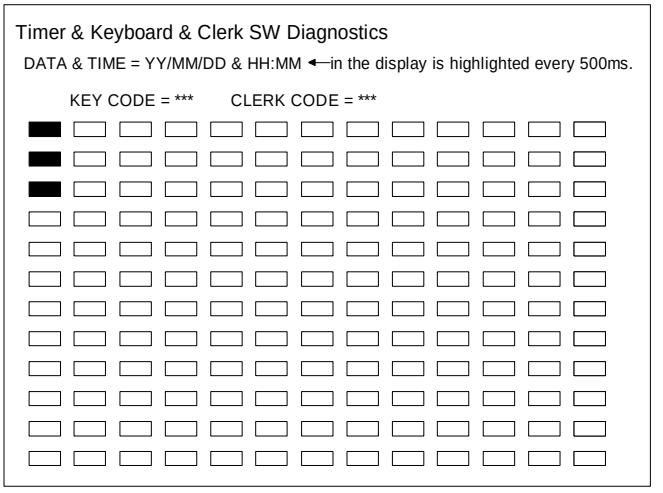
③ Terminating procedure

After displaying the check result, press the CANCEL key to terminate the check.

3-4. Timer & Keyboard & Clerk Switch Diagnostics

The operation of the clock crystal of CKDC, the keyboard, and the clerk switch are tested.

When the CANCEL key is pressed, the display returns to the diagnostics menu.


Timer & Keyboard & Clerk SW Diagnostics
DATA & TIME = YY/MM/DD & HH:MM ←in the display is highlighted every 500ms.
KEY CODE = ***
CLERK CODE = ***

1) Timer Check

① Check content

The operation of the clock crystal of CKDC7 is checked.

"YY/MM/DD & MM:HH" in the display is highlighted every 500ms. Check the highlighted display.

2) Keyboard Check

① Check content

The A750 main body keyboard input test is performed. The position code corresponding to the inputted key is displayed in three digits. The key layout corresponding to the input is displayed on the LCD screen. Press the corresponding key to input. The display of the inputted key is changed from white square □ to black square ■ and a catch sound is generated.

3) Clerk SW Check

① Check content

The code of the key which is inserted into the clerk key switch is displayed in a decimal number.

3-5. RS232 I/F Diagnostics

The main PWB and the option PWB (RS232 interface of ER-A7RS) are checked. Attach the 9-pin D-Sub loop back connector (UKOG-6717RCZZ) of wiring in Fig. 3-11.

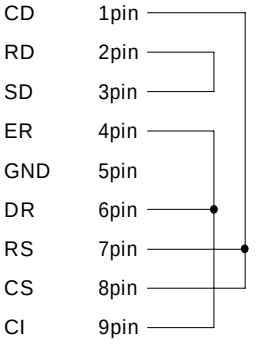


Fig. 3-11. Wiring diagram of loop back connector (UKOG-6717RCZZ)

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the CANCEL key is pressed, the display returns to the diagnostics menu.

When setting channels of RS232, do not set two or more ports to one channel. In the ER-A750, max. two units of ER-A7RS can be installed. In each PWB, do not set two or more ports to the same channel. If two or more ports should be set to one channel, the hardware would be destroyed.

```
RS232 I/F Diagnostics

   CHANNEL Check
   CH1 Check
   CH2 Check
   CH3 Check
   CH4 Check
   CH5 Check
   CH6 Check
   CH7 Check
```

1) CHANNEL Check

① Check content

The CHANNEL setting of the connected RS232 is displayed. The display content and the setting of DIP SW for CHANNEL setting on the RS232 I/F PWB are compared.

Since the RS232 on the main PWB of the ER-A750 is fixed to CH1 and CH2, that in the ER-A7RS must be set to CH3 ~ CH7.

```
RS232 I/F Diagnostics

   CHANNEL Check
   CH1 = exist!     ← Display when channel present
   CH2 = exist!
   CH3 = none!      ← Display when no channel
   CH4 = none!
   CH5 = none!
   CH6 = none!
   CH7 = none!
```

(Reference) ER-A7RS CHANNEL setting (In the table below, "1" = SW OFF, "0" = SW ON.)

ER-A7RS CON2

S1-1	S1-2	S1-3	CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Impossible to set
0	1	0	CHANNEL 2: Impossible to set
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6
1	1	1	CHANNEL 7

ER-A7RS CON3

S1-4	S1-5	S1-6	CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Impossible to set
0	1	0	CHANNEL 2: Impossible to set
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6
1	1	1	CHANNEL 7

② Terminating procedure

Press the CANCEL key to terminate the check.

2) CH1 Check

① Check content

When the channel is not set, an error display is made (ERROR:CH1). When the channel is set, the following check is performed.

- Control signal check

ERn	RSn	DRn	CIn	CDn	CSn
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check of the above inputs and the interruption check of CS, CI, and CD are performed.

In the read check, ER and RS are changed over in the above sequence and the logic states of DR, CI, CD, and CS are checked.

If the logic differs from that in the table, an error display is made.

"ON" in the table means Active LOW, and "OFF" means Active HIGH.

In the interruption check, an interruption of CS, CI, or CD is allowed one by one. (MASK is canceled.)

If an interruption is not made when each signal is active, or if an interruption is made when each signal is not active, an error display is made.

The above check is repeated four cycles.

- Data transfer check

The loop back data (256 bytes) of 00H ~ 0FFH are used for data transfer check. The baud rate is set to 38400BPS.

- Timer check (RS232 on board timer)

Before performing the check, set the timer to TCVDT start and 5ms. Then perform the following procedure.

∗ During execution of the check, TRQ- must not be generated.

∗ After 5ms from completion of the check, TRQ- must be generated.

② Display

```
RS232 CH1 Check

ER-DR          :     ERROR!!
```

All the contents of an error must be displayed.

ERROR No.	ERROR display	ERROR content
1	ER-DR:ERROR	ER-DR LOOP ERROR
2	ER-CI:ERROR	ER-CI LOOP ERROR
3	RS-CD:ERROR	RS-CD LOOP ERROR
4	RS-CS:ERROR	RS-CS LOOP ERROR
5	CI INT:ERROR	CI interruption is not made.
6	CD INT:ERROR	CD interruption is not made.
7	CS INT:ERROR	CS interruption is not made.
8	TXEMP:ERROR	TXEMP is not set.
9	TXEMP INT:ERROR	TXEMP interruption is not made.
10	TXRDY:ERROR	TXRDY interruption is not made.
11	TXRDY INT:ERROR	TXRDY interruption is not made.
12	RCVRDY:ERROR	RCVRDY is not set. (Reception enabled. TR-Q is generated during check)
13	RCVRDY INT:ERROR	RCVRDY interruption is not made.
14	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR)
15	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR, FRAMING ERROR, etc.)
16	TIMER:ERROR	TIMER ERROR (TMRQ is not set after completion of check.)
17	TIMER INT:ERROR	TRQ-1 interruption is not made.

③ Terminating procedure

Press the CANCEL key to terminate the check.

3) CH2 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

4) CH3 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

5) CH4 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

6) CH5 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

7) CH6 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

8) CH7 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

3-6. Liquid Crystal Display Diagnostics

The ER-A750 LCD display is checked.

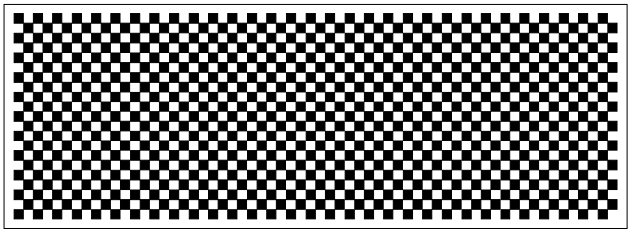
The test program displays the patterns in the following sequence. Every time when the ENTER key is pressed, the next pattern is displayed. When the ENTER key is pressed at the final pattern, or when the CANCEL key is pressed at the midst of the check, the display returns to the menu screen.

1) Liquid Crystal Display Check

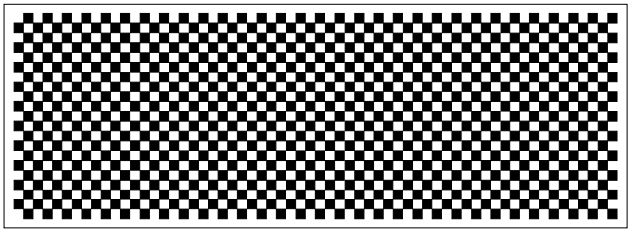
① Check content

The test patterns are displayed in the following sequence. When the ENTER key is pressed, the next pattern is displayed.

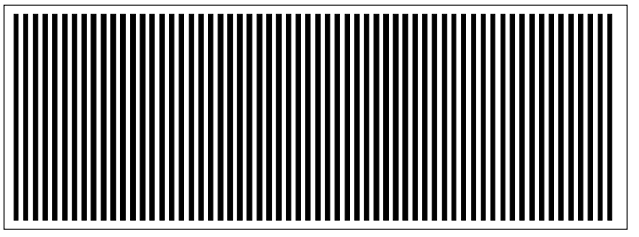
- Black and white pattern at 1 dot pitch



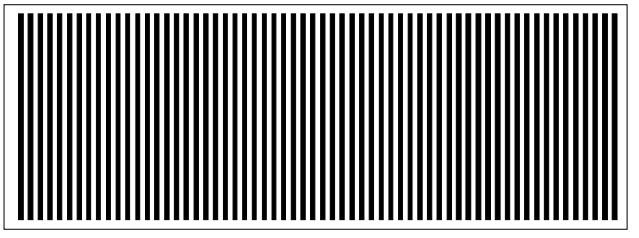
- Reversed pattern of the above



- Vertical stripe pattern at 1 dot pitch

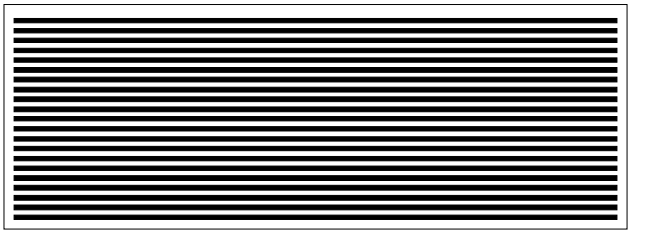


- Reversed pattern of the above

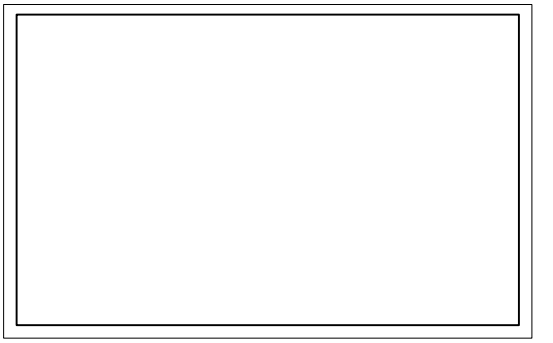


- Horizontal stripe pattern at 1 dot pitch

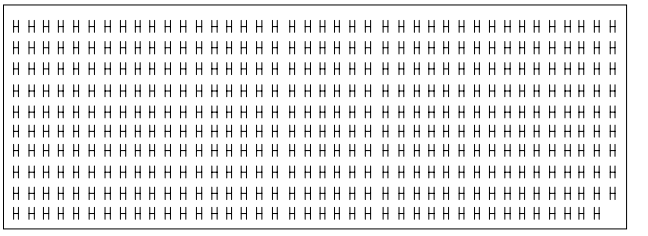
- Reversed pattern of the above



- The outermost peripheral of the LCD's active area is displayed in one-dot line.



- "H" pattern. "H" is displayed in 40 digits and 15 lines. The 15th line only has 39 digits of "H."



③ Terminating procedure

Press the ENTER key at the final pattern, or press the CANCEL key to terminate the check.

3-7. Rear Display Diagnostics

The rear display is checked.

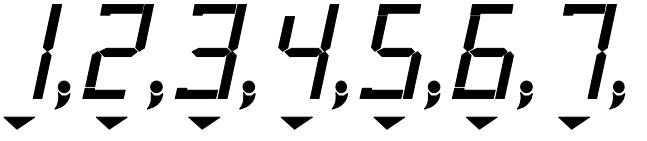
The test program displays the following patterns. When the CANCEL key is pressed, the display returns to the diagnostics menu.

1) Rear Display Check

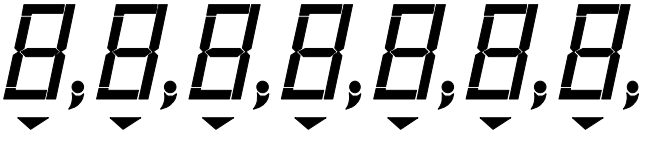
① Check content

The test patterns are displayed in the following sequence. When the ENTER key is pressed, the next pattern is displayed.

- The test pattern below is displayed.



- The test pattern with all the elements ON is displayed.



② Display

```
Rear Display Check
```

③ Terminating procedure

Press the CANCEL key to turn off all the elements of the rear display.

3-8. SHARP Retail Network Diagnostics

The SRN test is performed.

To perform this test, the following composition is required.

- ER-A750
- Terminal resistor
- Branch (trunk) cable (only for data transfer test)

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the individual diagnostics program is completed, the display returns to this menu screen. When the CANCEL key is pressed, the display returns to the diagnostics menu.

```
SRN Diagnostics

   Self Check
   Flag Send Check
   Data Send Check
   Data Check (Satellite Machine)
   Data Check (Master Machine)
```

1) SRN Self Check

① Check content

The ROM and RAM for SRN are checked, and CTC interruption and carrier sense are checked. Also ADLC function and transmission/reception DMA check is made by using the self loop function of ADLC (MC6854). In addition, the other signals are checked. The check procedure is as follows:

- Execute diagnostics command 2. The number of resending is displayed.
- Execute diagnostics command 0. The error status is displayed. The error status is as shown in the table below. When an error occurs in this test, the following tests are not performed.

b7	An error occurs. (The error print is always 1.)
b6	An unexpected interruption is made.
b5	A collision is generated.
b4	An interruption of send complete cannot be made. (DMAC TC UP interruption)
b3	An interruption of carrier OFF cannot be made. The mirror image of carrier OFF shows carrier ON.
b2	An interruption of CTC CH2 or CH3 cannot be made. (Timer interruption)
b1	ROM sum check error
b0	TAM error

- Execute diagnostics command 1. The error status is displayed. The error status is as shown in the table below.

b7	An error is generated. (The error print is always 1.)
b6	An unexpected interruption is generated.
b5	DMA sent data and received data are different.
b4	The number of data received in DMA is abnormal.
b3	The number of data transmitted in DMA is abnormal.
b2	An overrun error is generated.
b1	An underrun error is generated.
b0	An interruption of send complete cannot be made. (DMAC TC UP interruption)

- Execute diagnostics command 5. The error status is displayed. The names and the directions of the signals which are subject to diagnostics 5 command are as shown in the table below.

Signal name	Direction
Power interruption notice	Host → Controller
Power interruption ON initialization	Host → Controller
Power interruption ON continuation	Host → Controller
Power interruption process complete	Host ← Controller
CH1 reception data present.	Host ← Controller
CH2 reception data present.	Host ← Controller

Check that the target bit of two statuses obtained by diagnostics 5 command is "0" for ST1 and "1" for ST2. (The other bits must be masked.) In the other cases, the error status is displayed with the error occurrence bit as "1." The normal bit shows "0."

The error status from the host to the controller is as shown in the table below.

b7	Not used. ("0" is always displayed.)
b6	Power interruption notice
b5	Not used. ("0" is always displayed.)
b4	Not used. ("0" is always displayed.)
b3	Not used. ("0" is always displayed.)
b2	Not used. ("0" is always displayed.)
b1	Power ON continuation
b0	Power ON initializing

The error status from the controller to the host is as shown in the table below.

b7	Not used. ("0" is always displayed.)
b6	Power interruption notice
b5	Not used. ("0" is always displayed.)
b4	CH2 reception data exits.
b3	CH1 reception data exits.
b2	Power interruption process complete
b1	Not used. ("0" is always displayed.)
b0	Not used. ("0" is always displayed.)

② Display

```
SRN Self Check
   DATA RETRY CNT.=xxx  ┐
   ACK  RETRY CNT.=xxx  ┘ The number of resending is displayed in xxx with a decimal number.
   DIAG 0       :xxxxxxxx— In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
   DIAG 1       :xxxxxxxx— In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
   DIAG 5 H→C   :xxxxxxxx— In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
   DIAG 5 H←C   :xxxxxxxx— In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
```

③ Terminating procedure

Press the CANCEL key to terminate the check. After terminating, perform the service reset.

2) SRN Flag Send Check

① Check content

Execute diagnostics 3 command to send Flag (7EH) continuously.

② Display

```
SRN Flag Send Check
```

③ Terminating procedure

Perform the service reset.

3) SRN Data Send Check

① Check content

Execute diagnostics 4 command to send data of 00H ~ FFH (256Byte) as one packet at 12.8msec packet interval at 1Mbps continuously.

② Display

```
SRN Data Send Check
```

③ Terminating procedure

Perform the service reset.

4) Data Transmission Check

Data transmission is checked in an actually composed system. The system is composed of one master machine and max. 15 satellite machines.

Note for starting the check

- When checking the set in which the SRN setting has been made, cancel the SRN setting before starting this check.
- When checking the actually composed system, disconnect the SRM cables of the sets which are not checked, or cancel the SRN setting. If it is set to "SRN exits," data may be destroyed.
- The transmission check setting must be performed after canceling the SRN setting of all the sets in the system. First, set the satellite machines, then set the master machine.

① Setting procedure

- Satellite machine setting

  In the menu screen, select "Data Transmission Check (Satellite)."

  The display is as follows:

```
Data Transmission Check (Satellite)

   Input Terminal Number  :
```

Enter the terminal No. (000 ~ 254, 3 digits) of the machine to be checked and press the ENTER key. The display is as shown below.

```
Data Transmission Check (Satellite)

   Input Terminal Number : xxx     – The entered
   Data Sequence Number  : 0000      terminal No. is
                                     displayed.
```

- Master machine setting

  In the menu screen, select "Data Transmission Check (Master Machine)." The display is as shown below.

```
Data Transmission Check (Master)

   Input Master Terminal Number  :
```

Enter the terminal No. (000 ~ 254, 3 digits) of the machine to be checked and press the ENTER key. The display is as shown below.

```
Data Transmission Check (Master)

   Input Master Terminal Number    : xxx – The entered
   Input Satellite Terminal Number:        terminal No.
                                           is displayed.
```

Enter the terminal No. (000 ~ 254, 3 digits) of the machine to be connected to the machine to be checked and press the ENTER key. The display is as shown below.

```
Data Transmission Check (Master)

   Input Master Terminal Number    : xxx
   Input Satellite Terminal Number: xxx – The entered
                                          terminal No.
                                          of satellite
                                          machine is
                                          displayed.
```

When checking with two or more satellite machines connected, enter the terminal No. (000 ~ 254, 3 digits) and press the ENTER key similarly. To execute, press the ENTER key without entering the terminal No. The display is as shown below. Do not use the same terminal No. for different machines (master/satellite).

```
Data Transmission Check (Master)

   Input Master Terminal Number    : xxx
   Input Satellite Terminal Number : xxx
   xxx xxx xxx xxx xxx

   Data Sequence Number            : 0000
```

With the above setting, data transmission between the master machine and the satellite machine is started.

② Check content

- Data in the following format composed of 2byte sequence No. and 254byte AAH data are transmitted from the master machine to the satellite machine. The master machine displays the sequence No.

1	2	3	4	5	···	···	···	254	255	256	Byte
XX	XX	AA	AA	AA	···	···	···	AA	AA	AA	

XXXX : Sequence No. (2byte: 4digits of binary decimal numbers)
AA : Transmission data (AAH) x 254 bytes

- The satellite machine sends back the received data to the master machine. The satellite machine displays the received sequence No.
- The master machine receives the data, and checks the sequence No. and 256byte AAH data. In case of an error, the master machine displays an error code and terminates the check. If two or more satellite machines are used, the above operation is repeated. If data transmission with all the satellite machines are normally completed, the master machine increments the sequence No.

The above operation is repeated.

③ Error display

```
Data Transmission Check (Master)

   Input Master Terminal Number     : xxx
   Input Satellite Terminal Number : xxx
   xxx xxx xxx xxx xxx

   Data Sequence Number             : xxxx
   IRC Error                        : xx — The error code is displayed.
```

The error codes are as shown below.

01	Command abnormality (except for during transmission)
02	No data received.
03	Received data present. Received data remained.
04	Remote station not ready (in sending) "NTDY" is sent back because the remote station is not ready for reception.
05	Reception buffer full (in sending) The controller reception buffer of the remote machine is full.
06	Resend error (in sending) Retry over (5 times) when no response
07	Collision error (in sending) When an collision occurred in data transmission, retry over (16 times) at re-collision after a random time (0 ~ 255ms).
08	Line busy time out Transmission cannot be made by multi-station communication to cause time out in data send wait time.
09	Reception size over (in receiving) The reception buffer size is insufficient.
0A	Hardware error Interface abnormality (No SRN interface or abnormality in SRN controller)

③ Terminating procedure

Press the CANCEL key to terminate the check. After terminating, perform the service reset.

3-9. IrDA & ASK Diagnostics

This is used to check the IR communication.

To execute this check, the following composition is required.

- ER-A750
- ER-A750 as checker

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the CANCEL key is pressed, the display returns to the diagnostics menu.

```
IR (IrDA & ASK) Diagnostics

   IrDA & ASK Check
   IrDA & ASK Check (CHECKER MODE)
   Data Transmission Check (Receive MODE)
   Data Transmission Check (Send MODE)
```

1) IrDA & ASK Check

IR communication is checked between the ER-A750 sending unit and the receiving unit.

① Check content

- Data transmission is made from the machine to be checked in ASK format. The transmission rate is 9600bps. Data of 00H, 11H, 22H, 33H, 44H, 55H, 66H, 77H, 88H, 99H, AAH, BBH, CCH, EEH, and FFH are transmitted.
- The checker machine sends back the received data.
- The machine to be checked compares the data sent back and the data transmitted first. If both data are the same, it displays "PASS !!," and if not the same, "ERROR !!."
- Data transmission is made from the machine to be checked in IrDA format. The transmission rate is 9600bps. Data of 00H, 11H, 22H, 33H, 44H, 55H, 66H, 77H, 88H, 99H, AAH, BBH, CCH, EEH, and FFH are transmitted.
- The checker machine sends back the received data.
- The machine to be checked compares the data sent back and the data transmitted first. If both data are the same, it displays "PASS !!," and if not the same, "ERROR !!."

② Display

```
IrDA & ASK Check
DATA (or TIMEOUT) :  PASS!!(or ERROR!!)
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

2) IrDA & ASK Check (checker mode)

Set the checker machine (ER-A750) corresponding to the above check content (1).

② Display

```
IrDA & ASK Check (CHECKER MODE)
DATA (or TIMEOUT) :  PASS!!(or ERROR!!)
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

3) Data Transmission Check (Receive mode)

① Check content

Continuous IR communication between the ER-A750 and the ER-A750. This mode is on the reception side. When data of 256byte (00H ~ 0FFH) are received, data packet counter is incremented by one. Check that the counter increments.

② Display

```
Data Transmission Check (Receive MODE)
COUNTER : **** (The RING COUNTER (0~9999) is displayed.)
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

4) Data Transmission Check (Send mode)

① Check content

Continuous IR communication between the ER-A750 and the ER-A750. This mode is on the transmission side. When data of 256byte (00H ~ 0FFH) are transmitted, data packet counter is incremented by one. Check that the counter increments.

② Display

```
Data Transmission Check (Send MODE)
COUNTER : **** (The RING COUNTER (0~9999) is displayed .)
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

3-10. Magnetic Card Reader Diagnostics

Read check of the optional ER-A8MR + ER-A7RS is performed.

The test program reads the magnetic card of ISO 7811/1-5 standard and displays the data. When the CANCEL key is pressed, the display returns to the diagnostics menu.

1) Magnetic Card Reader Check

① Check content

The test program reads tracks 1 and 2 of the magnetic card of ISO 7811/1-5, and displays the data in ASCII code.

② Display

```
  MCR (Magnetic Card Reader) Check

    TRACK1:
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxxxxx
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
    TRACK2:
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

XXXXX shows the data read by the MCR. Incase of an error, the error code is displayed as shown below.

```
Magnetic Card Reader Check

   TRACK1:BUFFER EMPTY  – Displayed when TRACK1 empty
                          code is sent back.
   TRACK1:MCR ERROR     – Displayed when TRACK1 error
                          code is sent back.
   TRACK2:BUFFER EMPTY  – Displayed when TRACK2 empty
                          code is sent back
   TRACK2:MCR ERROR     – Displayed when TRACK2 error
                          code is sent back.
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

3-11. Drawer Diagnostics

This diagnostics is used to check the drawer open and sensors.

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the CANCEL key is pressed, the display returns to the diagnostics menu.

```
Drawer Diagnostics
   Drawer 1 Check
   Drawer 2 Check
```

1) Drawer 1 Check

① Check content

The solenoid of drawer 1 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

② Display

```
Drawer 1 Check
   Drawer Open Sensor  :  OPEN (or CLOSE)
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

2) Drawer 2 Check

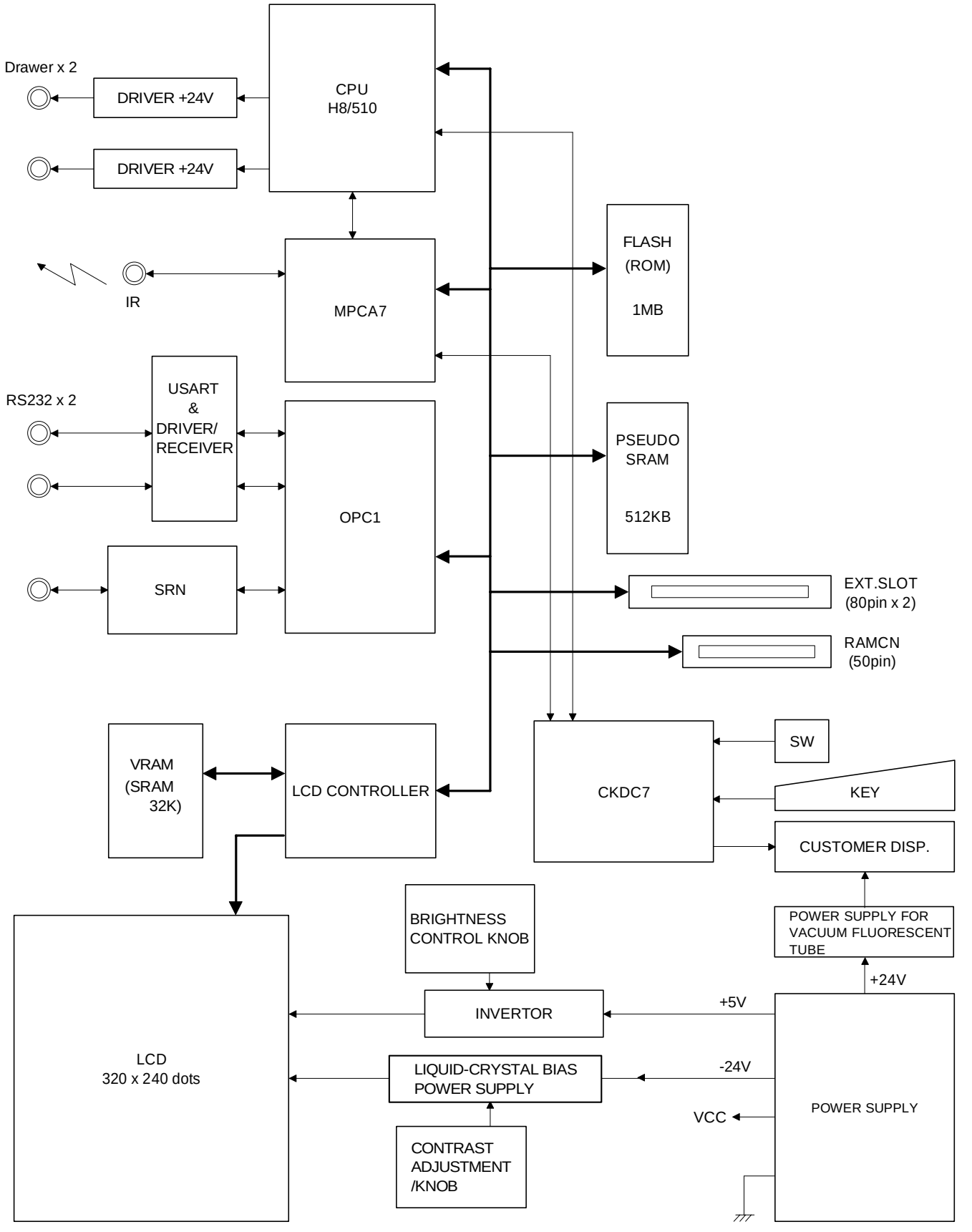
① Check content

The solenoid of drawer 2 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

The display and the terminating procedure are the same as Drawer 1 Check.

CHAPTER 7. CIRCUIT DESCRIPTION

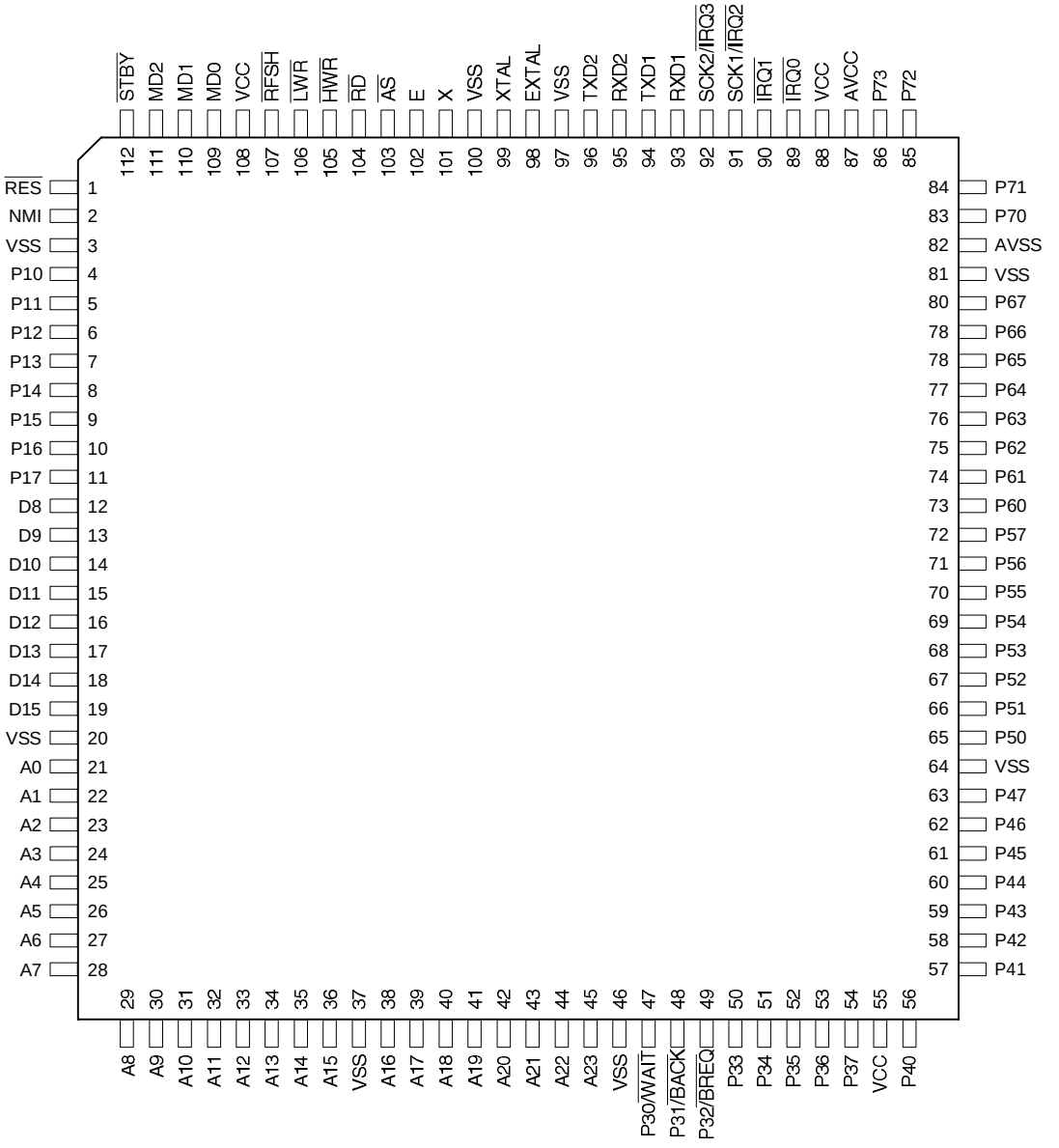
1. Hardware block diagram



2. Description of main LSI's

2-1. CPU (HD6415108FX)

1) Pin configuration



HD6415108FX pin configuration

Fig. 2-1

2) Block diagram

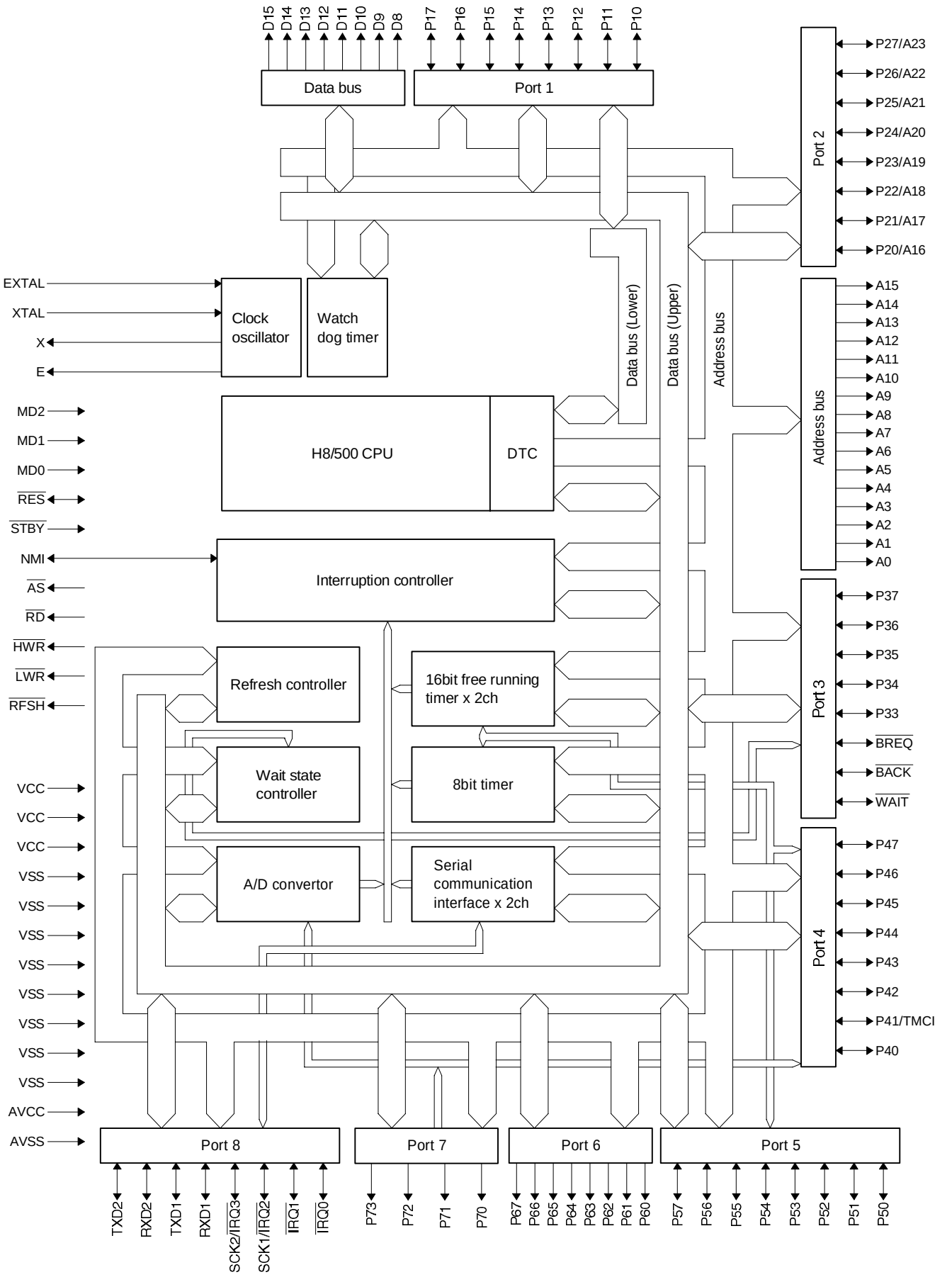


Fig. 2-2

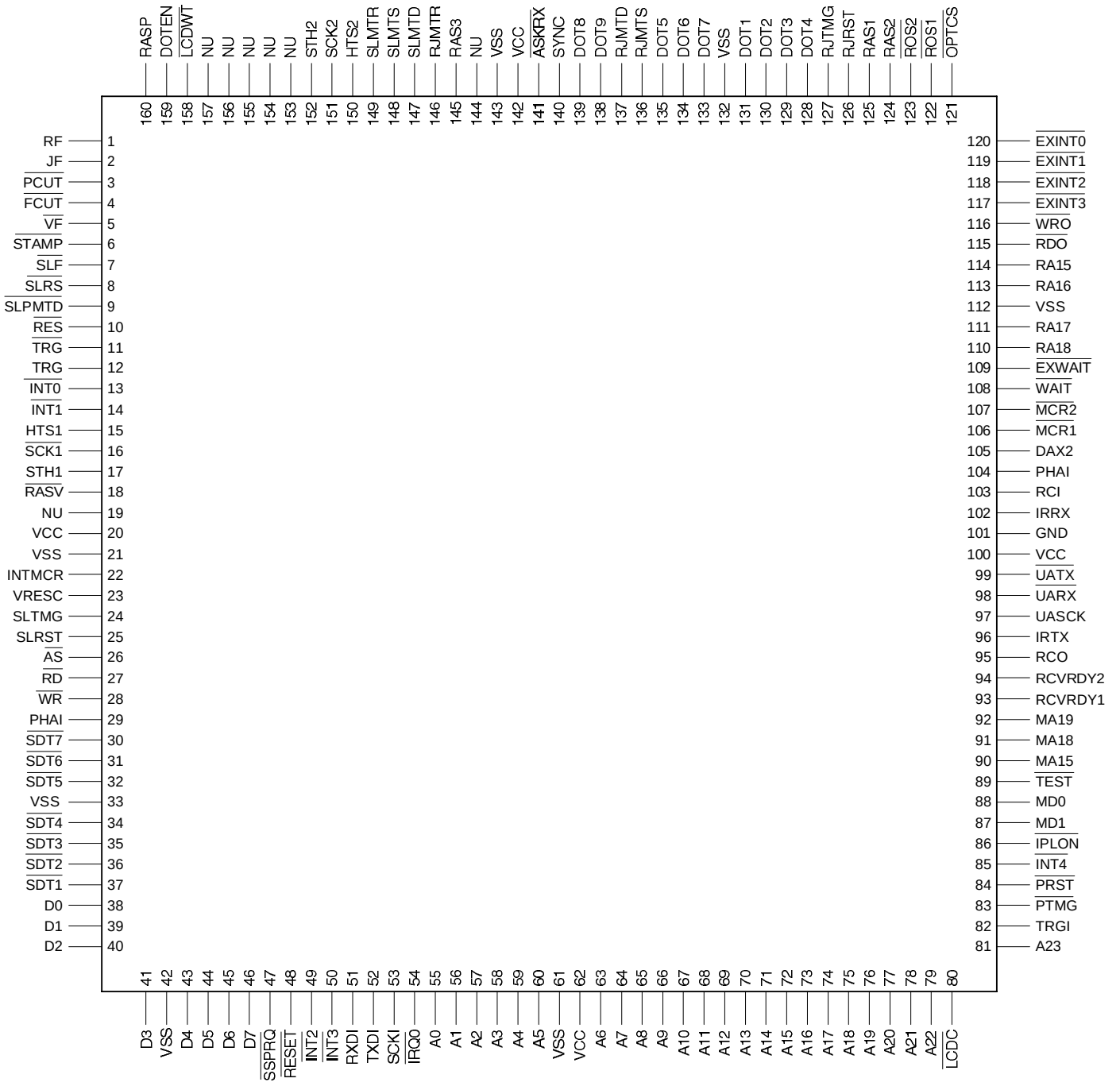
3) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	$\overline{RES}$	$\overline{RESET}$	I/O	Reset input
2	NMi	NMi	In	Non-maskable interrupt input for SSP interrupt input.
3	VSS	NU	In	GND
4	P10	$\overline{IPLON0}$	In	IPLON signal for factory setting (from expansion I/O port)
5	P11	$\overline{PNLSNS}$	In	IPLON signal for servicing
6	P12	$\overline{IPLON2}$	In	LCD sensing signal at main PWB side
7	P13	NORDY	In	Flash memory RY/BY # signal
8	P14	FVPON	Out	Flash memory write protect signal output
9	P15	BKLT	Out	Backlight control signal
10	P16	Nu	In	GND
11	P17	MVDT	In	Memory version detect
12	D8	D0	I/O	Data bus
13	D9	D1	I/O	Data bus
14	D10	D2	I/O	Data bus
15	D11	D3	I/O	Data bus
16	D12	D4	I/O	Data bus
17	D13	D5	I/O	Data bus
18	D14	D6	I/O	Data bus
19	D15	D7	I/O	Data bus
20	VSS	NU	In	GND
21	A0	A0	Out	Address bus
22	A1	A1	Out	Address bus
23	A2	A2	Out	Address bus
24	A3	A3	Out	Address bus
25	A4	A4	Out	Address bus
26	A5	A5	Out	Address bus
27	A6	A6	Out	Address bus
28	A7	A7	Out	Address bus
29	A8	A8	Out	Address bus
30	A9	A9	Out	Address bus
31	A10	A10	Out	Address bus
32	A11	A11	Out	Address bus
33	A12	A12	Out	Address bus
34	A13	A13	Out	Address bus
35	A14	A14	Out	Address bus
36	A15	A15	Out	Address bus
37	VSS	NU	In	GND
38	A16	A16	Out	Address bus
39	A17	A17	Out	Address bus
40	A18	A18	Out	Address bus
41	A19	A19	Out	Address bus
42	A20	A20	Out	Address bus
43	A21	A21	Out	Address bus
44	A22	A22	Out	Address bus
45	A23	A23	Out	Address bus
46	VSS	NU	In	GND
47	P30	$\overline{WAIT}$	In	Wait signal
48	P31	$\overline{BACK}$	Out	Bus control request acknowledge
49	P32	$\overline{BREQ}$	In	Bus control request
50	P33	DOPS	In	Drawer open signal
51	P34	$\overline{DR0}$	Out	Option drawer open signal
52	P35	$\overline{DR1}$	Out	Remote drawer No.1 open signal
53	P36	NU	Out	NU
54	P37	NU	Out	NU
55	VCC	VCC	In	+5V

Pin No.	Symbol	Signal name	In/ Out	Function
56	P40	VCC	In	+5V
57	P41	NU	In	GND
58	P42	NU	In	GND
59	P43	NU	In	GND
60	FTi1/P44	INTMCR	In	MCR interrupt signal
61	P45	NU	In	GND
62	FTi2/P46	$\overline{SHEN}$	In	CKDC Interface shift enable signal
63	P47	NU	In	GND
64	VSS	VSS	In	GND
65	P50	NU	Out	GND
66	P51	NU	Out	GND
67	P52	NU	Out	GND
68	P53	NU	In	GND
69	P54	NU	Out	GND
70	P55	NU	In	GND
71	P56	NU	Out	GND
72	P57	$\overline{STOP}$	Out	System reset output. Normally
73	P60	NU	Out	GND
74	P61	NU	In	GND
75	P62	NU	In	GND
76	P63	NU	In	GND
77	P64	NU	Out	GND
78	P65	NU	Out	GND
79	P66	NU	In	GND
80	P67	NU	In	GND
81	VSS	NU	In	GND
82	AVSS	NU	In	GND
83	P70	NU	In	GND
84	P71	NU	In	GND
85	P72	NU	In	GND
86	P73	NU	In	GND
87	AVCC	AVCC	In	+5V
88	VCC	VCC	In	+5V
89	$\overline{IRQ0}$	$\overline{IRQ0}$	In	Interrupt signal 0
90	$\overline{IRQ1}$	$\overline{IRQ1}$	In	Interrupt signal 1
91	SCK1/$\overline{IRQ2}$	UASCK	In	Synchronizing shift lock signal for IR
92	SCK2	SCKi	In	CKDC Interface sync shift clock
93	RXD1	$\overline{UARX}$	In	RXD signal for IR
94	TXD1	$\overline{UATX}$	Out	TXD signal for IR
95	RXD2	RXDi	In	CKDC Interface shift input data
96	TXD2	TXDi	Out	CKDC Interface shift output data
97	VSS	NU	In	GND
89	EXTAL	EXTAL	In	Crystal oscillator connection
99	XTAL	XTAL	In	Crystal oscillator connection
100	VSS	NU	In	GND
101	X	#	Out	System clock
102	E	NU	Out	Nu
103	$\overline{AS}$	$\overline{AS}$	Out	Address strobe
104	$\overline{RD}$	$\overline{RD}$	Out	Read
105	$\overline{HWR}$	$\overline{WR}$	Out	Write
106	$\overline{LWR}$	$\overline{LWR}$	Out	Nu
107	$\overline{RFSH}$	$\overline{RFSH}$	Out	Refresh cycle
108	VCC	VCC	In	+5V
109	MD0	MD0	In	+5V (MODE 3)
110	MD1	MD1	In	+5V (MODE 3)
111	MD2	MD2	In	GND
112	$\overline{STBY}$	$\overline{STBY}$	In	+5V (Nu)

2-2. G.A (MPCA7)

1) Pin configuration



GATE ARRAY (LZ9AH30)
MPCA7

Fig. 2-3

2) Block diagram

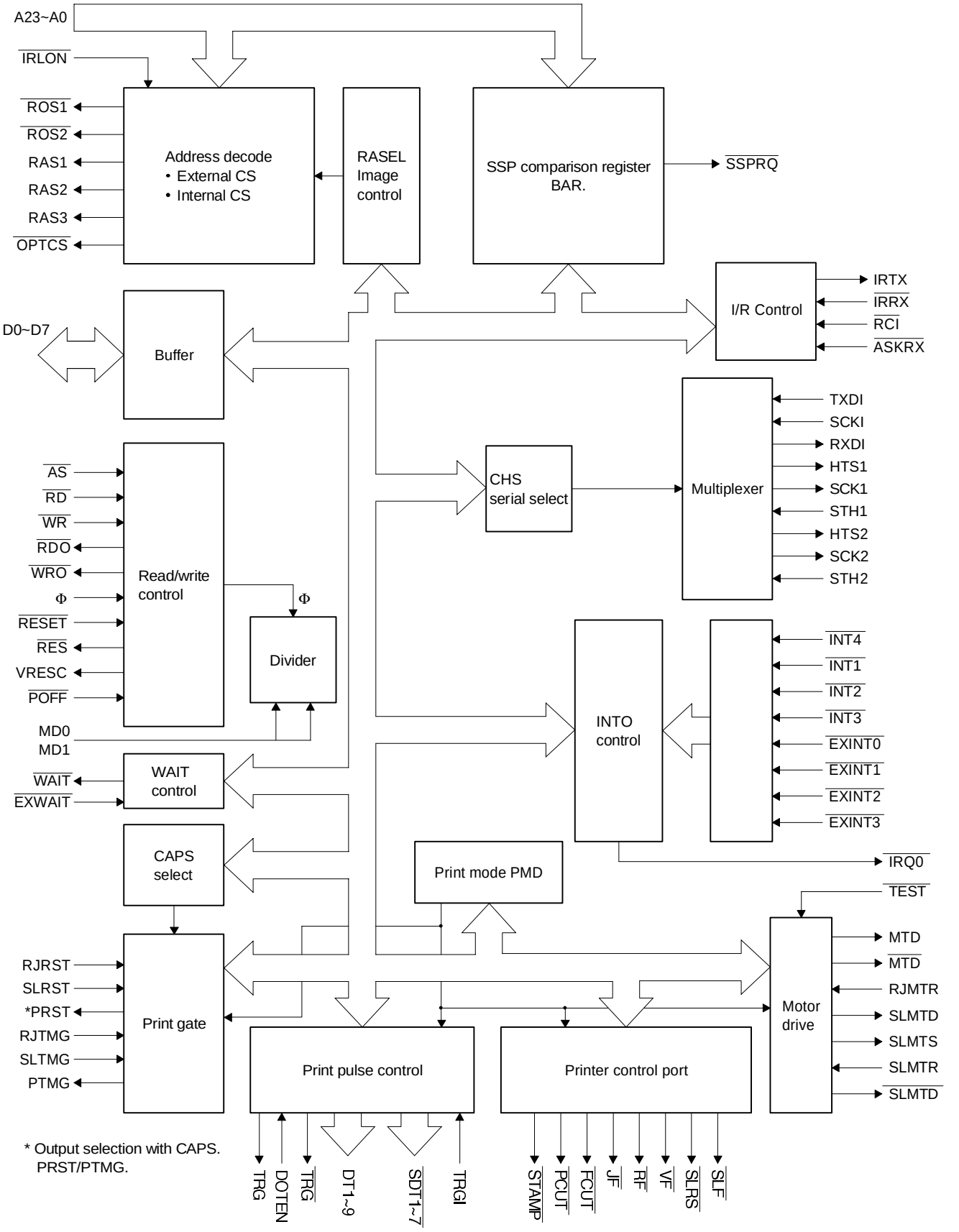


Fig. 2-4

3) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	RF	Nu	—	Nu
2	JF	Nu	—	Nu
3	$\overline{\text{PCUT}}$	Nu	—	Nu
4	$\overline{\text{FCUT}}$	Nu	—	Nu
5	$\overline{\text{VF}}$	Nu	—	Nu
6	$\overline{\text{STAMP}}$	Nu	—	Nu
7	$\overline{\text{SLF}}$	Nu	—	Nu
8	$\overline{\text{SLRS}}$	Nu	—	Nu
9	$\overline{\text{SLPMTD}}$	Nu	—	Nu
10	$\overline{\text{RES}}$	$\overline{\text{RES}}$	Out	Peripheral output reset
11	$\overline{\text{TRG}}$	Nu	—	Nu
12	TRG	Nu	—	Nu
13	$\overline{\text{INT0}}$	$\overline{\text{POFF}}$	In	Power off signal input
14	$\overline{\text{INT1}}$	$\overline{\text{KRQ}}$	In	Interrupt signal (Key interrupt request)
15	HTS1	HTS	Out	8 bit serial port output
16	$\overline{\text{SCK1}}$	SCK	Out	Serial port shift clock output
17	STH1	STH	In	8 bit serial port input
18	$\overline{\text{RASV}}$	$\overline{\text{RASV}}$	Out	Chip select
19	Nu	Nu	—	Nu
20	VCC	VCC	—	+5V
21	VSS	GND	—	GND
22	INTMCR	INTMCR	Out	Interrupt signal (MCR)
23	VRESC	VRESC	In	Turns active when reset and power down is met
24	SLTMG	GND	—	GND
25	SLRST	GND	—	GND
26	$\overline{\text{AS}}$	$\overline{\text{AS}}$	In	Address strobe
27	$\overline{\text{RD}}$	$\overline{\text{RD}}$	In	Read strobe
28	$\overline{\text{WR}}$	$\overline{\text{WR}}$	In	Write strobe
29	PHAI	#	In	(ϕ) System clock (9.83MHz)
30	$\overline{\text{SDT7}}$	Nu	—	Nu
31	$\overline{\text{SDT6}}$	Nu	—	Nu
32	$\overline{\text{SDT5}}$	Nu	—	Nu
33	VSS	GND	—	GND
34	$\overline{\text{SDT4}}$	Nu	—	Nu
35	$\overline{\text{SDT3}}$	Nu	—	Nu
36	$\overline{\text{SDT2}}$	Nu	—	Nu
37	$\overline{\text{SDT1}}$	Nu	—	Nu
38	D0	D0	I/O	Data bus
39	D1	D1	I/O	Data bus
40	D2	D2	I/O	Data bus
41	D3	D3	I/O	Data bus
42	VSS	GND	—	GND
43	D4	D4	I/O	Data bus
44	D5	D5	I/O	Data bus
45	D6	D6	I/O	Data bus
46	D7	D7	I/O	Data bus
47	$\overline{\text{SSPRQ}}$	NMI	Out	SSP interrupt request to CPU
48	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	In	MPCA reset
49	$\overline{\text{INT2}}$	VCC	—	+5V
50	$\overline{\text{INT3}}$	VCC	—	+5V
51	RXDI	RXDI	Out	8 bit serial port output to CPU
52	TXDI	TXDI	In	8 bit serial port input from CPU
53	SCK1	SCK1	In	Serial port shift clock input from CPU

Pin No.	Symbol	Signal name	In/ Out	Function
54	$\overline{\text{IRQ0}}$	$\overline{\text{IRQ0}}$	Out	Interrput request to CPU
55	A0	A0	In	Address bus
56	A1	A1	In	Address bus
57	A2	A2	In	Address bus
58	A3	A3	In	Address bus
59	A4	A4	In	Address bus
60	A5	A5	In	Address bus
61	VSS	GND	—	GND
62	VCC	VCC	—	+5V
63	A6	A6	In	Address bus
64	A7	A7	In	Address bus
65	A8	A8	In	Address bus
66	A9	A9	In	Address bus
67	A10	A10	In	Address bus
68	A11	A11	In	Address bus
69	A12	A12	In	Address bus
70	A13	A13	In	Address bus
71	A14	A14	In	Address bus
72	A15	A15	In	Address bus
73	A16	A16	In	Address bus
74	A17	A17	In	Address bus
75	A18	A18	In	Address bus
76	A19	A19	In	Address bus
77	A20	A20	In	Address bus
78	A21	A21	In	Address bus
79	A22	A22	In	Address bus
80	$\overline{\text{LCDC}}$	$\overline{\text{LCDC}}$	Out	LCDC chip select signal
81	A23	A23	In	Address bus
82	TRGI	GND	In	GND
83	$\overline{\text{PTMG}}$	Nu	—	Nu
84	$\overline{\text{PRST}}$	Nu	—	Nu
85	$\overline{\text{INT4}}$	VCC	—	+5V
86	$\overline{\text{IPLON}}$	$\overline{\text{IPLON0}}$	In	To option connector
87	MD1	GND	—	GND
88	MD0	GND	—	GND
89	$\overline{\text{TEST}}$	VCC	—	+5V
90	MA15	MA15	Out	Image address 15
91	MA18	Nu	—	Nu
92	MA19	Nu	—	Nu
93	RCVRDY1	MCRRDY1	In	
94	RCVRDY2	MCRRDY2	In	
95	RCO	Nu	—	Nu
96	IRTX	IRTX	Out	I/R output for LED
97	UASCK	UASCK	Out	I/R serial data shift clock
98	$\overline{\text{UARX}}$	$\overline{\text{UARX}}$	Out	I/R serial data for CPU
99	$\overline{\text{UATX}}$	$\overline{\text{UATX}}$	In	I/R serial data from CPU
100	VCC	VCC	—	+5V
101	VSS	GND	—	GND
102	IRRX	IRDA	In	I/R input from IR unit
103	RCI	GND	—	GND
104	PHAI	PHAI	In	System clock (7.3728MHz)
105	DAX2	PHAI	In	System clock (7.3728MHz)
106	$\overline{\text{MCR1}}$	$\overline{\text{MCR1}}$	Out	
107	$\overline{\text{MCR2}}$	$\overline{\text{MCR2}}$	Out	
108	$\overline{\text{WAIT}}$	$\overline{\text{WAIT}}$	Out	Wait request signal
109	$\overline{\text{EXWAIT}}$	$\overline{\text{EXWAIT}}$	In	External wait control input signal

Pin No.	Symbol	Signal name	In/ Out	Function
110	RA18	Nu	—	Nu
111	RA17	Nu	—	Nu
112	VSS	GND	—	GND
113	RA16	Nu	—	Nu
114	RA15	Nu	—	Nu
115	$\overline{\text{RDO}}$	$\overline{\text{RDO}}$	Out	Expansion RD signal (Option)
116	$\overline{\text{WRO}}$	$\overline{\text{WRO}}$	Out	Expansion WR signal (Option)
117	$\overline{\text{EXINT3}}$	$\overline{\text{TRQ2}}$	In	Expansion interrupt signal (Option)
118	$\overline{\text{EXINT2}}$	$\overline{\text{TRQ1}}$	In	Expansion interrupt signal (OPC1)
119	$\overline{\text{EXINT1}}$	$\overline{\text{EXINT1}}$	In	Expansion interrupt signal (Option)
120	$\overline{\text{EXINT0}}$	$\overline{\text{EXINT0}}$	In	Expansion interrupt signal (Option)
121	$\overline{\text{OPTCS}}$	$\overline{\text{OPTCS}}$	Out	Chip select base siganal for expansion option
122	$\overline{\text{ROS1}}$	$\overline{\text{ROS1}}$	Out	ROM 1 chip select signal
123	$\overline{\text{ROS2}}$	$\overline{\text{ROS2}}$	Out	ROM 2 chip select signal
124	RAS2	Nu	—	Nu
125	RAS1	Nu	—	Nu
126	RJRST	GND	—	GND
127	RJTMG	GND	—	GND
128	DOT4	Nu	—	Nu
129	DOT3	Nu	—	Nu
130	DOT2	Nu	—	Nu
131	DOT1	Nu	—	Nu
132	VSS	GND	—	GND
133	DOT7	Nu	—	Nu
134	DOT6	Nu	—	Nu
135	DOT5	Nu	—	Nu
136	RJMTS	Nu	—	Nu
137	RJMTD	Nu	—	Nu
138	DOT9	Nu	—	Nu
139	DOT8	Nu	—	Nu
140	SYNC	SYNC	In	
141	$\overline{\text{ASKRX}}$	ASK	In	I/R input from IR unit
142	VCC	VCC	—	+5V
143	VSS	VSS	—	GND
144	NU	Nu	—	Nu
145	RAS3	RAS3	Out	RAM3 chip select signal
146	RJMTR	GND	—	GND
147	SLMTD	Nu	—	Nu
148	SLMTS	Nu	—	Nu
149	SLMTR	GND	—	GND
150	HTS2	Nu	—	Nu
151	SCK2	Nu	—	Nu
152	STH2	VCC	—	+5V
153	NU	Nu	—	Nu
154	NU	Nu	—	Nu
155	NU	Nu	—	Nu
156	NU	Nu	—	Nu
157	NU	Nu	—	Nu
158	LCDWT	LCDWT	In	LCDC wait signal
159	DOTEN	NU	—	NU
160	RASP	RASP	Out	Standard RAM chip select signal

2-3. OPC1 (F256004PJ)

1) General description

The OPC1 is a gate array of integrated peripheral circuits of RS-232/Simple IRC interface.
One chip of the OPC1 is equipped with four communication circuits. (Three of them are for RS-232 only: UNIT 0 ~ 2, one is for selection of simple IRC/RS-232: UNIT 3)
The ER-A750 uses UNIT0 (RS-232 interface) and UNIT7 (RS-232 interface).

UNIT NO.	Purpose	ER-A750
UNIT0	RS-232	Used.
UNIT1	RS-232	Used.
UNIT2	RS-232	Not used.
UNIT3	RS-232/IRC	Not used.

Each UNIT of the OPC1 has the following functions:

① Timer function
Used for the timer between characters in data reception.

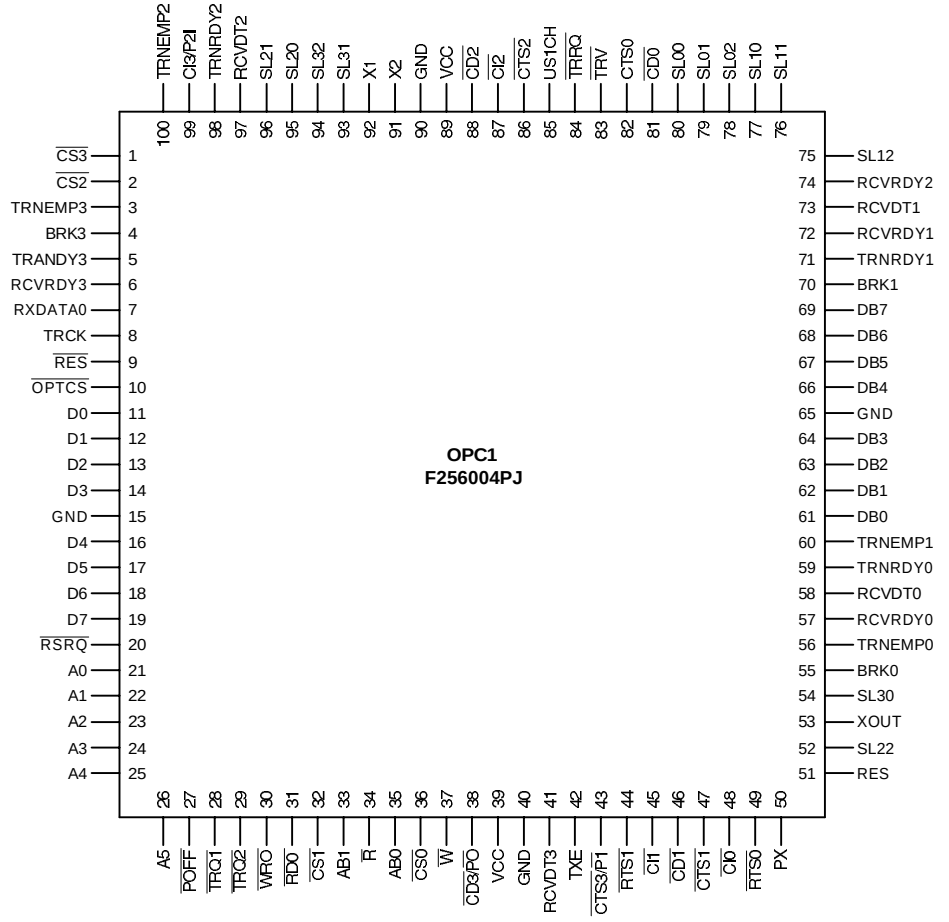
② Address decode
USART chip select output and own select.

③ Interruption control
$\overline{\text{RSRQ}}$, $\overline{\text{TRRQ}}$ output using outputs from USART (TRNRDY, TRNEMP, RCVRDY, BRK) and RS-232 control signals ($\overline{\text{CI}}$, $\overline{\text{CTS}}$, $\overline{\text{CD}}$) as interruption factors.
(For the simple IRC, TRNEMP is excluded.)

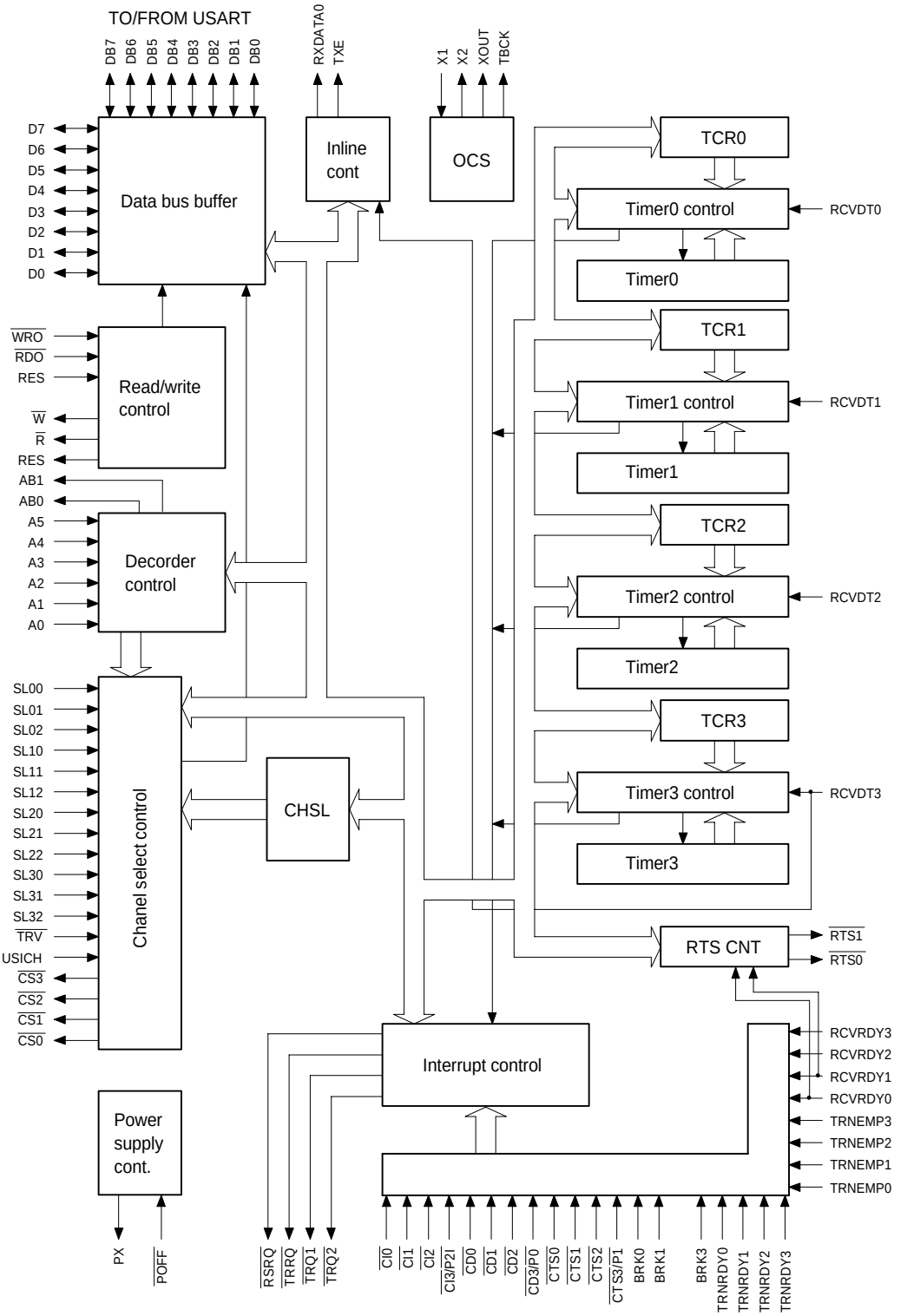
✳ $\overline{\text{RSRQ}}$: For RS-232
$\overline{\text{TRRQ}}$: For IRC

④ Simple IRC send/receive control (UNIT3 only) : Not used

2) Pin configuration



3) Block diagram



4) Pin description

OPC1 pin table

The signals marked with "-" at the end are LOW active signals. Example: "CS1-" = "$\overline{CS1}$"

No.	Pin No.	Pin name	I/O	Pin	ER-A750	Description
1	80	SL00	I	ICU	+5V	RS-232/UNIT0 channel select
2	79	SL01	I	ICU	GND	
3	78	SL02	I	ICU	GND	
4	77	SL10	I	ICU	GND	RS-232/UNIT1 channel select
5	76	SL11	I	ICU	+5V	
6	75	SL12	I	ICU	GND	
7	95	SL20	I	ICU	GND	RS-232/UNIT2 channel select
8	96	SL21	I	ICU	GND	
9	52	SL22	I	ICU	GND	
10	54	SL30	I	ICU	GND	RS-232/UNIT3 channel select
11	93	SL31	I	ICU	GND	
12	94	SL32	I	ICU	GND	
13	36	CS0-	O	O	CS1-	RS-232 USART chip select
14	32	CS1-	O	O	CS2-	
15	2	CS2-	O	O	NC	
16	1	CS3-	O	O	$\overline{SRCS}$	RS-232/INLINE USART chip select
17	81	CD0-	I	IS	DCD1-	RS-232 control signal CD- input
18	46	CD1-	I	IS	DCD2-	
19	88	CD2-	I	IS	+5V	
20	38	CD3-/P0-	I	IS	$\overline{SINT}$	RS-232 CD-/INLINE P0-
21	82	CTS0-	I	IS	CTS1-	RS-232 control signal CTS- input
22	47	CTS1-	I	IS	CTS2-	
23	86	CTS2-	I	IS	+5V	
24	43	CTS3-/P1-	I	IS	GND	RS-232 CTS-/INLINE P1-
25	48	CI0-	I	IS	CI1-	RS-232 control signal CI- input
26	45	CI1-	I	IS	CI2-	
27	87	CI2-	I	IS	+5V	
28	99	CI3-/P2I	I	IS	GND	RS-232 CI-/INLINE P2I
29	55	BRK0	I	ISC	BRK1	RS-232 USART BREAK signal
30	70	BRK1	I	ISC	BRK2	
31	27	POFF-	I	IS	POFF-	POFF signal (LOW: P-OFF, HIGH: P-ON)
32	4	BRK3	I	IS	GND	RS-232/INLINE USART BREAK signal
33	57	RCVRDY0	I	ISC	RCVRDY1	RS-232 USART RCVRDY signal
34	72	RCVRDY1	I	ISC	RCVRDY2	
35	74	RCVRDY2	I	ISC	GND	
36	6	RCVRDY3	I	IS	GND	RS-232/INLINE USART RCVRDY signal
37	59	TRNRDY0	I	ISC	TRNRDY1	RS-232 USART TRNRDY signal
38	71	TRNRDY1	I	ISC	TRNRDY2	
39	98	TRNRDY2	I	ISC	GND	
40	5	TRNRDY3	I	IS	GND	RS-232/INLINE USART TRNRDY signal
41	56	TRNEMP0	I	ISC	TRNEMP1	RS-232 USART TRNEMP signal
42	60	TRNEMP1	I	ISC	TRNEMP2	
43	100	TRNEMP2	I	ISC	GND	
44	3	TRNEMP3	I	IS	+5V	RS-232/INLINE USART TRNEMP signal
45	58	RCVDT0	I	ISC	RCVDT1	RS-232 RCVDT signal (LOW: TIMER START)
46	73	RCVDT1	I	ISC	RCVDT2	
47	97	RCVDT2	I	ISC	+5V	
48	41	RCVDT3	I	IS	GND	RS-232/INLINE RCVDT signal
49	20	RSRQ-	O	3S	RSRQ-	RS-232 IRQ- signal
50	83	TRV-	I	ISC	GND	INLINE YES/NO
51	7	RXDATA0	O	O	NC	INLINE RXDATA OUT
52	42	TXE	O	O	$\overline{SRESET}$	INLINE TRNS ENABLE
53	84	TRRQ-	O	3S	$\overline{TRQ2}$	INLINE IRQ- signal
54	28	TRQ1-	O	3S	$\overline{TRQ1}$	TIMER IRQ signal (RS-232)

No.	Pin No.	Pin name	I/O	Pin	ER-A750	Description
55	29	TRQ2-	O	3S	NC	TIMER IRQ signal (INLINE)
56	11	D0	I/O	IOU	D0	DATA BUS (MAIN)
57	12	D1	I/O	IOU	D1	
58	13	D2	I/O	IOU	D2	
59	14	D3	I/O	IOU	D3	
60	16	D4	I/O	IOU	D4	
61	17	D5	I/O	IOU	D5	
62	18	D6	I/O	IOU	D6	
63	19	D7	I/O	IOU	D7	
64	61	DB0	I/O	IOU	DB0	DATA BUS (USART)
65	62	DB1	I/O	IOU	DB1	
66	63	DB2	I/O	IOU	DB2	
67	64	DB3	I/O	IOU	DB3	
68	66	DB4	I/O	IOU	DB4	
69	67	DB5	I/O	IOU	DB5	
70	68	DB6	I/O	IOU	DB6	
71	69	DB7	I/O	IOU	DB7	
72	21	A0	I	I	A0	ADDRESS BUS (MAIN)
73	22	A1	I	I	A1	
74	23	A2	I	I	A2	
75	24	A3	I	I	A3	
76	25	A4	I	I	A4	
77	26	A5	I	I	A5	
78	10	OPTCS-	I	I	OPTCS-	OPTION CHIP SELECT (from MPCA7)
79	31	RDO-	I	I	RDO-	READ signal (from MPCA7)
80	30	WRO-	I	I	WRO-	WRITE signal (from MPCA7)
81	9	RES-	I	IS	RES-	RESET signal (from MAIN)
82	34	R-	O	O	$\overline{\text{RDH}}$	READ signal (To USART)
83	37	W-	O	O	$\overline{\text{WRH}}$	WRITE signal (To USART)
84	51	RES	O	O	RES USART	RESET signal (To USART)
85	92	X1	O		NC	cillation circuit
86	91	X2	I		#	
87	53	XOUT	O	O	CLK USART	Clock for USART
88	8	TRCK	O	O	NC	T/R clock for 1CH USART
89	35	AB0	O	O	AH0	Address bus for USART
90	33	AB1	O	O	AH1	
91	85	USICH	I	ISC	GND	UNIT3 USART 1CH/2CH select
92	50	PX		O	NC	Power source clock
93	39	VCC			+5V	
94	89	VCC			+5V	
95	15	GND			GND	
96	40	GND			GND	
97	65	GND			GND	
98	90	GND			GND	
99	49	RTS0-	O	O	RTS1-	RS-232 control signal RTS- output
100	44	RTS1-	O	O	RTS2-	

ICU : CMOS level input (internal pullup resistor)
O : Output
IS : TTL level input (internal schmit circuit)
ISC : CMOS level input (internal schmit circuit)
3S : Three state output
IOU : I/O port (internal pullup resistor)

2-4. USART (MB89371A)

1) General

The MB89371A (Serial data transmitter/receiver, 2 units) is a versatile-use interface LSI for communication lines, which is equipped with two sets of equivalent units of the MB89251A (serial data transmitter/receiver), the baud rate generating section, and the interruption adjustment section.

It is positioned between the line Modem and the computer, and used for serial/parallel conversion of data, data send/receive operation check, and the synchronization mode selection according to the program assignment.

The transmitter section converts parallel data into serial data, and adds the parity bit, the start bit, and the stop bit to them, and transmits them. In the synchronization mode, it transmits synchronization characters during no transmission data period. In the advancement synchronization mode, it allows selection of transmission clocks and transmission baud rates.

The receiving section converts serial data into parallel data, and checks parities to judge that data are properly transmitted.

In the synchronization mode, it detects synchronization characters and makes synchronization of transmission/reception operations with the transmitter side. In the advancement synchronization mode, it allows selection of transmission clocks and reception baud rates.

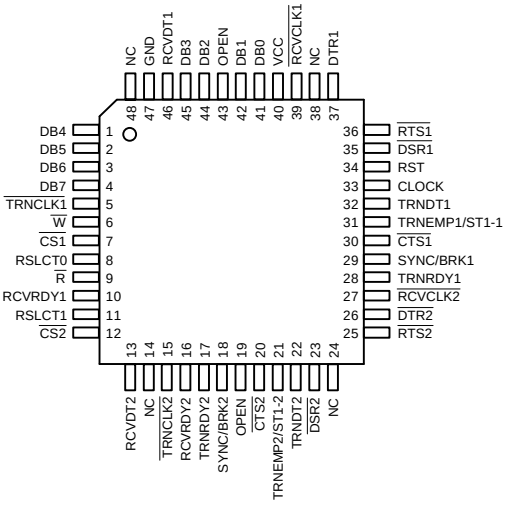
The baud rate generating section generates clock pulse signals which are used in transmission and reception and delivered through the baud rate selecting section to the SDTR section.

It provides the loop back diagnostic function which crosses interface lines of the Modem and loops transmission and reception signals, facilitating the operation check.

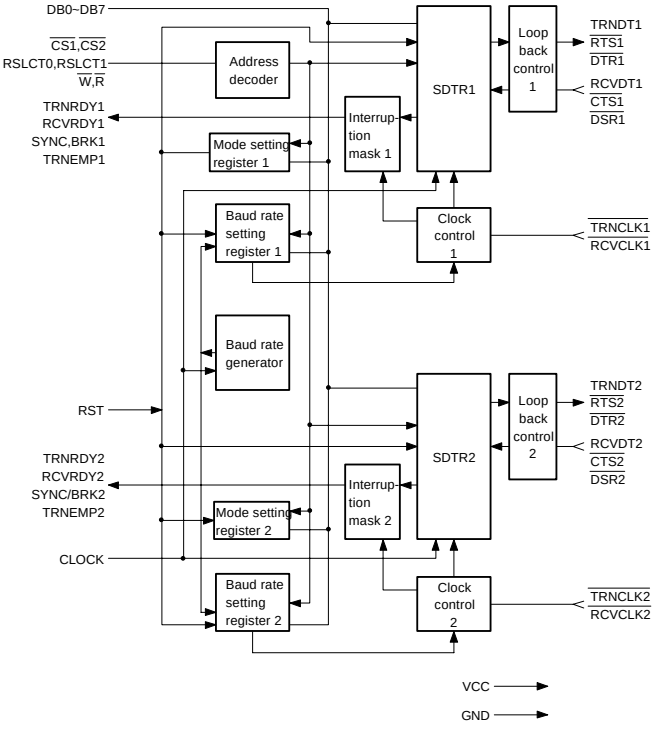
Features

- Two independent channels of SDTR.
- Built-in baud rate generator which allows setting for each channel
- External clock available
- Internal clock output available.
- Maskable interruption generating circuit
- Two channels are assigned to different address spaces.
- Baud rate DC ~ 240K baud (with external clocks)
- Full duplex communication
- Program assignment in synchronization mode
  - Data bit length: 5 - 8 bits
  - Character synchronization system: Internal synchronization, external synchronization
  - Number of synchronized characters: Single character, double characters
  - Parity occurrence and check: parity valid/invalid
even parity, odd parity
- Operations in the synchronization mode
  - Overrun error and parity error detection
  - Transmit/receive buffer state acknowledgment
  - Synchronization character detection
  - Automatic insertion of synchronization character
- Program assignment function in the advancement synchronization mode
  - Data bit length: 5 ~ 8 bits
  - Stop bit length: 1, 1½, 2 bits
  - Baud rate: Transmission clock, reception clock x 1, x 1/16, x 1/64
  - Parity occurrence and check: Parity valid, invalid
Even parity, odd parity
- Operations in the advancement synchronization mode
  - Detection of framing error, overrun error, parity error
  - Transmission/reception buffer state acknowledgment
  - Break characters detection
- Error start bit detection
- IBM Bi-sync system operation allowed.
- Duplex buffer system in the transmission and the reception sections.
- Loop back diagnostic functions
- I/O signal level TTL compatible
- Compatible with standard microprocessor in connecting pins and signal timing.
- Standard 42 pin plastic DIP, 48 pin plastic QFP
- +5V single power source

2) Pin configuration



3) Block diagram



4) Pin description

No.	Pin No.	Pin name	I/O	ER-A750	
1	1	DB4	I/O	DB4	Data bus
2	2	DB5	I/O	DB5	
3	3	DB6	I/O	DB6	
4	4	DB7	I/O	DB7	
5	41	DB0	I/O	DB0	
6	42	DB1	I/O	DB1	
7	44	DB2	I/O	DB2	
8	45	DB3	I/O	DB3	
9	46	RCVDT1	I	RCVDT1	RS-232 reception data signal
10	13	RCVDT2	I	RCVDT2	
11	47	GND	–	GND	
12	5	TRNCLK1-	I	GND	Data transmission clock
13	15	TRNCLK2-	I	GND	
14	6	W-	I	$\overline{\text{WRH}}$	Write signal
15	7	CS1-	I	CS1-	RS-232 chip select
16	12	CS2-	I	CS2-	
17	8	RSLCT0	I	AH0	Address bus
18	11	RSLCT1	I	AH1	
19	9	R-	I	$\overline{\text{RDH}}$	Read signal
20	10	RCVRDY1	O	RCVRDY1	RS-232 data reception enable signal
21	16	RCVRDY2	O	RCVRDY2	
22	28	TRNRDY1	O	TRNRDY1	RS-232 data transmission enable signal
23	17	TRNRDY2	O	TRNRDY2	
24	29	BRK1	O	BRK1	Break code detection signal
25	18	BRK2	O	BRK2	
26	30	CTS1-	I	(CTS1-)GND	RS-232 clear to send signal
27	20	CTS2-	I	(CTS2-)GND	
28	31	TRNEMP1	O	TRNEMP1	RS-232 transmission buffer empty signal
29	21	TRNEMP2	O	TRNEMP2	
30	14	NC	–	NC	
31	24	NC	–	NC	
32	38	NC	–	NC	
33	48	NC	–	NC	
34	19	OPEN		NC	
35	43	OPEN		NC	
36	32	TRNDT1	O	TXD1	RS-232 transmission data signal
37	22	TRNDT2	O	TXD2	
38	35	DSR1-	I	DSR1-	RS-232 data set ready signal
39	23	DSR2-	I	DSR2-	
40	36	RTS1-	O	NC	Request to send signal
41	25	RTS2-	O	NC	
42	37	DTR1-	O	DTR1-	RS-232 data terminal ready signal
43	26	DTR2-	O	DTR2-	
44	39	RCVCLK1-	I	GND	Data reception clock
45	27	RCVCLK2-	I	GND	
46	33	CLOCK	I	CLK USART	Clock signal
47	34	RST	I	RES USART	RESET signal
48	40	VCC	–	+5V	+5V

2-5. Z80 CPU

1) Features

The extensive instruction set contains 158 instructions, including the 8080A instruction set as a subset.

- NMOS version for low cost high performance solutions, CMOS version for high performance low power designs.
- Z0840006 - 6.17 MHz
- CMOS Z84C0006 - DC to 6.17 MHz, Z84C008 - DC to 8 MHz, Z84C0010 - DC to 10 MHz, Z84C0020 - DC - 20 MHz
- 6 MHz version can be operated at 6.144 MHz clock.
- The Z80 microprocessors and associated family of peripherals can be linked by a vectored interrupt system. This system can be daisy-chained to allow implementation of a priority interrupt scheme.
- Duplicate set of both general-purpose and flag registers.
- Two sixteen-bit index registers.
- Three modes of maskable interrupts:
  Mode 0 — 8080A similar;
  Mode 1 — Non-Z80 environment, location 38H;
  Mode 2 — Z80 family peripherals, vectored interrupts.
- On-chip dynamic memory refresh counter.

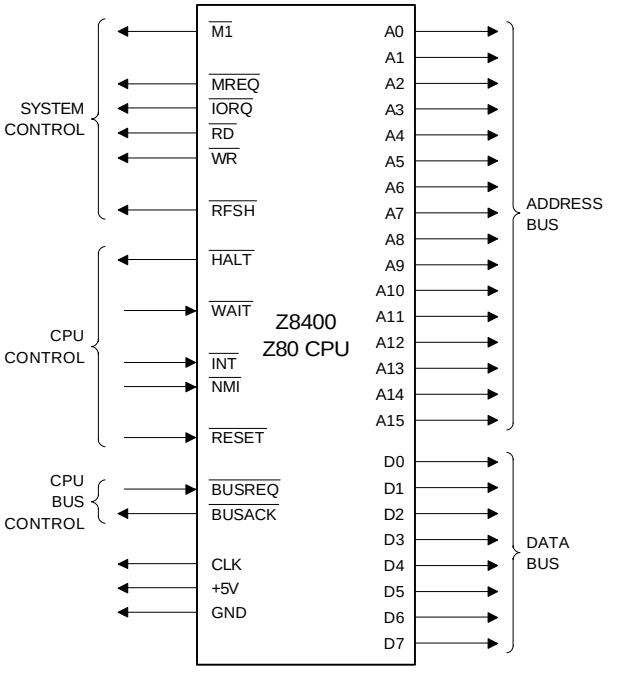
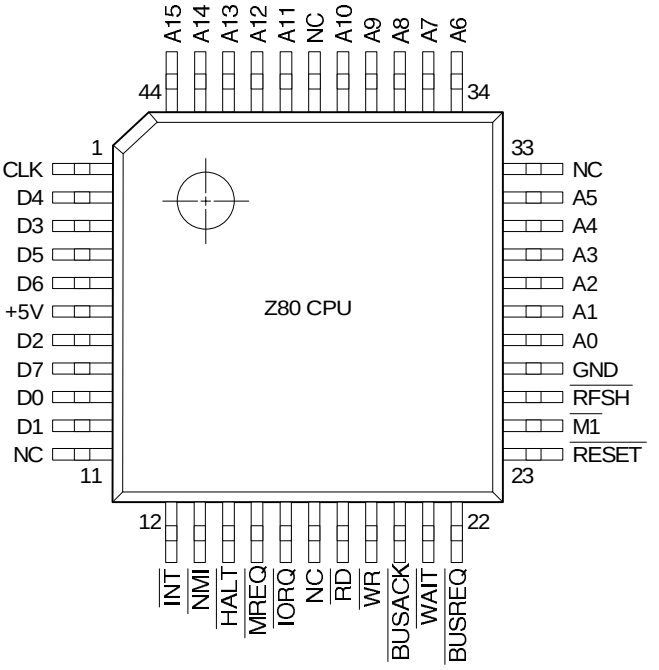


Figure 1. Pin functions

2) Pin configuration



44 pin Quad Flat Pack (QFP), Pin Assignments
(Only available for 84C00)

3) General description

The CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer.

These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

The internal block diagram (Figure 3) shows the primary functions of the processors. Subsequent text provides more detail on the I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

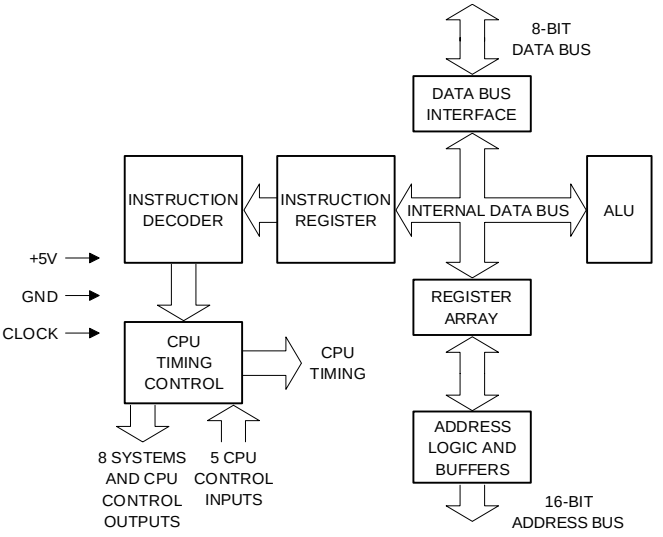


Figure 3. Z80C CPU Block Diagram

4) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	CLK	CLK	In	Clock
2	D4	S D4	In/Out	Data bus
3	D3	S D3	In/Out	Data bus
4	D5	S D5	In/Out	Data bus
5	D6	S D6	In/Out	Data bus
6	+5V	VCC	—	+5V
7	D2	S D2	In/Out	Data bus
8	D7	S D7	In/Out	Data bus
9	D0	S D0	In/Out	Data bus
10	D1	S D1	In/Out	Data bus
11	NC	NC	—	NC
12	$\overline{INT}$	S INT	In	Interrupt request signal
13	$\overline{NMI}$	VCC	—	Non-maskable interrupt signal
14	$\overline{HALT}$	VCC	—	+5V
15	$\overline{MREQ}$	S $\overline{MRQ}$	Out	Memory request signal
16	$\overline{IORQ}$	S $\overline{IORQ}$	Out	Input / Output request signal
17	NC	NC	—	NC
18	$\overline{RD}$	S $\overline{RDS}$	Out	Rread signal
19	$\overline{WR}$	S $\overline{WRS}$	Out	Write signal
20	$\overline{BUSAK}$	$\overline{BUSAK}$	Out	Bus acknowledge signal
21	$\overline{WAIT}$	S $\overline{WAIT}$	In	Wait signal
22	$\overline{BUSRQ}$	$\overline{BUSRQ}$	In	Bus request signal
23	$\overline{RESET}$	S $\overline{RES}$	In	Reset signal
24	$\overline{M1}$	S M1	Out	Machine cycle one signal
25	$\overline{RFSH}$	NC	—	NC
26	GND	GND	—	GND
27	A0	S A0	Out	Address bus
28	A1	S A1	Out	Address bus
29	A2	S A2	Out	Address bus
30	A3	S A3	Out	Address bus
31	A4	S A4	Out	Address bus
32	A5	S A5	Out	Address bus
33	NC	NC	—	NC
34	A6	S A6	Out	Address bus
35	A7	S A7	Out	Address bus
36	A8	S A8	Out	Address bus
37	A9	S A9	Out	Address bus
38	A10	S A10	Out	Address bus
39	NC	NC	—	NC
40	A11	S A11	Out	Address bus
41	A12	S A12	Out	Address bus
42	A13	S A13	Out	Address bus
43	A14	S A14	Out	Address bus
44	A15	S A15	Out	Address bus

2-6. Z80 CTC

1) Features

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors. (1.5mV @ 1.5V)
- NMOS version for cost sensitive performance solutions.
- CMOS version for the designs requiring low power consumption
- NMOS Z0843004 - 4 MHz, Z0843006 - 6.17 MHz.
- CMOS Z84C3006 - DC to 6.17 MHz, Z84C3008 - DC to 8 MHz, Z84C3010 - DC to 10 MHz
- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritaized interrupts without external logic. The CTC may also be used as an interrupt controller.
- 6 MHz version supports 6.144 MHz CPU clock operation.

2) General description

The Z80 CTC, hereinafter referred to as Z80 CTC or CTC, four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.
System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

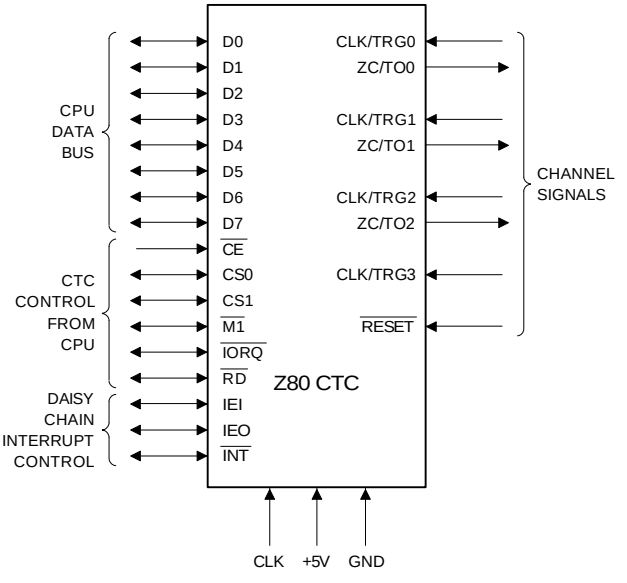


Figure 1. Pin Functions

Programming the CTC is straightforward: each channel is programmed with two bytes: a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified: the CTC internally generates a unique vector for each channel.
The Z80 CTC requires a single +5% V power supply and the standard Z80 single-phase system clock. It is packaged in 28-pin DIPs, a 44-pin plastic chip carrier, and a 44-pin Quad Flat Pack. (Figures 2a, 2b, and 2c). Note that the QFP package is only available for CMOS versions.

3) Pin configuration

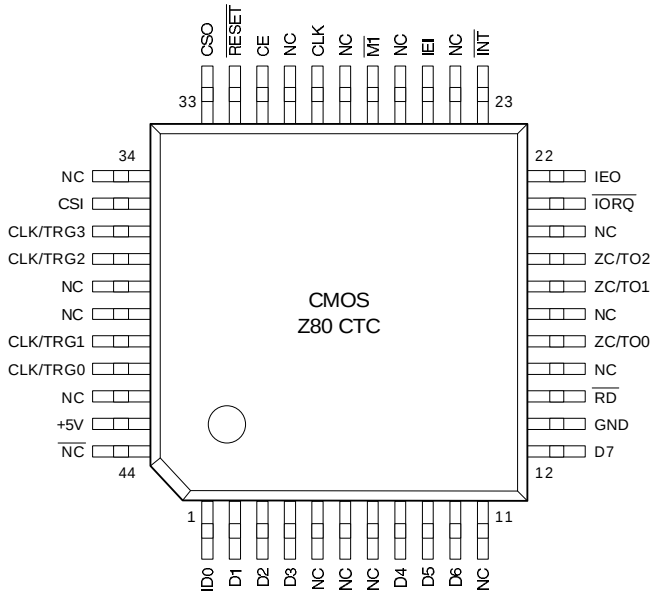


Figure 2c. 44-pin Quad Flat Pack Pin Assignments

4) Functional description

The Z80 CTC has four independent counter/timer channels. Each channel is individually programmed with two words: a control word and a time-constant word. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets a prescaler, which divides the system clock by either 16 or 256. The time-constant word is a value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode operation the counter decrements on each of the CLK/TRG input pulses until zero count is reached. Each decrement is synchronized by the system clock. For counts greater than 256, more than one counter can be cascaded. At zero count, the down-counter is automatically reset with the time constant value.

The timer mode determines time intervals as small as 2 μs (8 MHz), 3 μs (6 MHz), or 4 μs (4 MHz) without additional logic or software timing loops. Time intervals are generated by dividing the system clock with a prescaler that decrements a preset down-counter.

Thus, the time interval is an integral multiple of the clock period, the prescaler value (16 or 256), and the time constant that is preset in the down-counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

Three channels have two outputs that occur at zero count.

The first output is a zero-count/timeout pulse at the ZC/TO output. The fourth channel (Channel 3) does not have a ZC/TO output; interrupt request is the only output available from Channel 3.

The second output is Interrupt Request ($\overline{INT}$), which occurs if the channel has its interrupt enabled during programming. When the Z80 CPU acknowledges Interrupt Request, the Z80 CTC places an interrupt vector on the data bus.

The four channels of the Z80 CTC are fully prioritized and fit into four configuous slots in a standard Z80 daisy-chain interrupt structure. Channel 0 is the highest priority and Channel 3 the lowest. Interrupts can be individually enabled (or disabled) for each of the four channels.

5) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	D0	S D0	In/Out	Data bus
2	D1	S D1	In/Out	Data bus
3	D2	S D2	In/Out	Data bus
4	D3	S D3	In/Out	Data bus
5	NC	NC	—	NC
6	NC	NC	—	NC
7	NC	NC	—	NC
8	D4	S D4	In/Out	Data bus
9	D5	S D5	In/Out	Data bus
10	D6	S D6	In/Out	Data bus
11	NC	NC	—	NC
12	D7	S D7	In/Out	Data bus
13	GND	GND	—	GND
14	$\overline{RD}$	S $\overline{RDS}$	In	Read cycle status signal
15	NC	NC	—	NC
16	ZC/TO0	S TM0	Out	Zero count / Timeout signal
17	NC	NC	—	NC
18	ZC/TO1	NC	—	NC
19	ZC/TO2	NC	—	NC
20	NC	NC	—	NC
21	$\overline{IORQ}$	S IORQ	In	Input / Output request signal
22	IEO	NC	—	NC
23	$\overline{INT}$	S INT	Out	Interrupt request signal
24	NC	NC	—	NC
25	IEI	VCC	—	+5V
26	NC	NC	—	NC
27	$\overline{M1}$	S M1	In	Machine cycle one signal
28	NC	NC	—	NC
29	CLK	CLK	In	System clock
30	NC	NC	—	NC
31	$\overline{CE}$	S A6	In	Chip enable signal
32	$\overline{RESET}$	S $\overline{RES}$	In	Reset signal
33	CS0	S A0	In	Channelselect signal
34	NC	NC	—	NC
35	CS1	S A1	In	Channelselect signal
36	CLK/TRG3	S TM1	In	External clock / timer signal
37	CLK/TRG2	S TM0	In	External clock / timer signal
38	NC	NC	—	NC
39	NC	NC	—	NC
40	CLK/TRG1	S $\overline{INTS}$	In	External clock / timer signal
41	CLK/TRG0	VCC	In	+5V
42	NC	NC	—	NC
43	+5V	VCC	—	+5V
44	NC	NC	—	NC

2-7. μPD71037

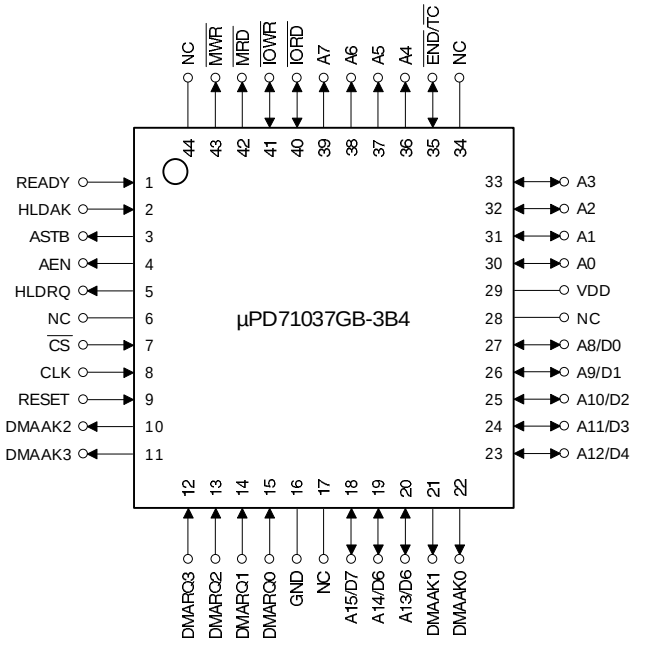
DMA CONTROLLER

The μPD71037 is a direct memory access controller (DMAC) for the micro processor system. It provides higher processing speed and lower power consumption in comparison with those in conventional use. Each of the four built-in DMA channels has 64-KB addresses and the function of counting the number of bytes of transferred data, and can transfer data from I/O to memory and from memory to memory as well.

1) FEATURES

- The clock speed is 10 MHz, twice that of the μPD8237A-5 (clock speed of 5 MHz).
- Each of the four DMA channels can be operated independently.
- Each channel can be self-initialized.
- Data is transferrable from memory to memory.
- Data in memory can independently initialized by block.
- High speed data transfer:
  3.2 MB/sec. (clock seed of 10 MHz, normal transfer mode)
  5.0 MB/sec. (clock speed of 10 MHz, compression transfer mode)
- The number of DMA channels can directly be expanded (Expansion mode).
- $\overline{\text{END}}$ input when data transfer is finished.
- Software DMA request available.
- CMOS
- Low power consumption

2) Pin configuration



3) Pin configuration

Pin No.	Symbol	Signal name	In/Out	Function
1	READY	READY	In	Ready signal
2	HLDAK	HLDAK	In	Hold acknowledge signal
3	ASTB	S ASTB	Out	Address strobe signal
4	AEN	S AEN	Out	Address enable signal
5	HLDRQ	HLDRQ	Out	Hold request signal
6	NC	NC	—	NC
7	$\overline{\text{CS}}$	$\overline{\text{CS}}$	In	Chip select signal
8	CLK	CLK	In	Clock
9	RESET	SRNRESET	In	Reset signal
10	DMAAK2	S DACK2	Out	DMA acknowlidge signal
11	DMAAK3	S DACK3	Out	DMA acknowlidge signal
12	DMARQ3	S DRQ3	In	DMA request signal
13	DMARQ2	S DRQ2	In	DMA request signal
14	DMARQ1	S DRQ1	In	DMA request signal
15	DMARQ0	S DRQ0	In	DMA request signal
16	GND	GND	—	GND
17	NC	NC	—	NC
18	A15/D7	S D7	In/Out	Data bus
19	A14/D6	S D6	In/Out	Data bus
20	A13/D6	S D5	In/Out	Data bus
21	DMAAK1	S DACK1	Out	DMA acknowlidge signal
22	DMAAK0	S DACK0	Out	DMA acknowlidge signal
23	A12/D4	S D4	In/Out	Data bus
24	A11/D3	S D3	In/Out	Data bus
25	A10/D2	S D2	In/Out	Data bus
26	A9/D1	S D1	In/Out	Data bus
27	A8/D0	S D0	In/Out	Data bus
28	NC	NC	—	NC
29	VDD	VCC	—	+5V
30	A0	S A0	In	Address bus
31	A1	S A1	In	Address bus
32	A2	S A2	In	Address bus
33	A3	S A3	In	Address bus
34	NC	NC	—	NC
35	$\overline{\text{END}}$ / $\overline{\text{TC}}$	TC	In/Out	End / Terminal cut signal
36	A4	S A4	In	Address bus
37	A5	S A5	In	Address bus
38	A6	S A6	In	Address bus
39	A7	S A7	In	Address bus
40	$\overline{\text{IORD}}$	S $\overline{\text{IOR}}$	In/Out	I/O read signal
41	$\overline{\text{IOWR}}$	S $\overline{\text{IOW}}$	In/Out	I/O write signal
42	$\overline{\text{MRD}}$	S $\overline{\text{MRD}}$	Out	Memory read signal
43	$\overline{\text{MWR}}$	NC	—	NC
44	NC	NC	—	NC

2-8. MB62H149

1) Outline

The MB62H149 is a semi-custom LSI chip for the peripheral circuits in the SRN (SHARP Retail Network), its main function is to communicate data with the host CPU and control the peripheral circuits and transmission control circuits of the Sub CPU (Z-80). Fig. 2. shows the general configuration of the functions:

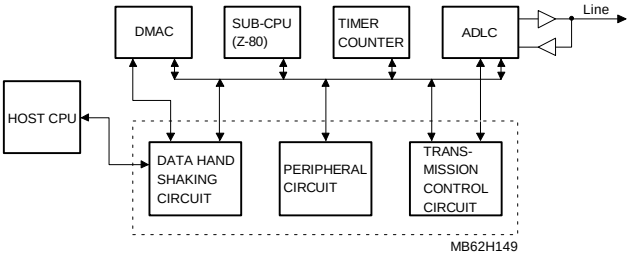


Fig. 2

2) Internal functions

(1) Data handshaking circuit

Is used because data processing speeds vary and the timing of the HOST CPU and SUB CPU do not synchronize, the MB62H149 is used for data handshaking. When the data handshaking portion is broken down, the system consists of a Write Signal from the HOST CPU to the MB62H149, Read Signal from the MB62H149 of the SUB CPU, Write Signal from the SUB CPU to the MB62H149 and Read Signal from the MB62H149 of the HOST CPU, all of which from two blocks as shown.

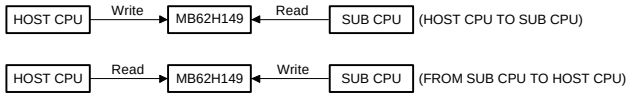


Fig. 3

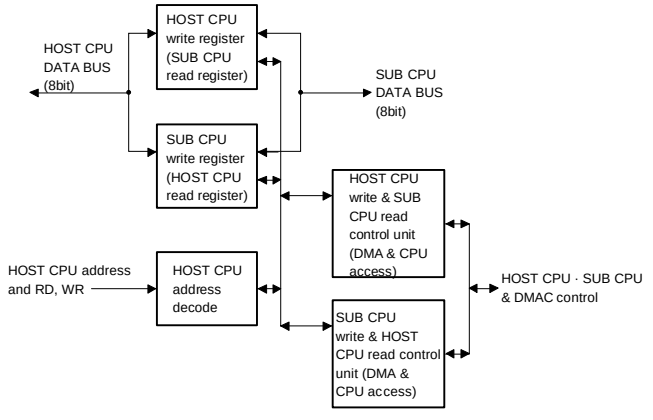

HOST CPU DATA BUS (8bit)
HOST CPU write register (SUB CPU read register)
SUB CPU DATA BUS (8bit)
SUB CPU write register (HOST CPU read register)
HOST CPU write & SUB CPU read control unit (DMA & CPU access)
HOST CPU address and RD, WR
HOST CPU address decode
HOST CPU · SUB CPU & DMAC control
SUB CPU write & HOST CPU read control unit (DMA & CPU access)

Fig. 4

(2) Peripheral circuit

The peripheral circuit consists of an I/O address generation unit on the SUB CPU, block dividing circuit, and the wait signal control unit.

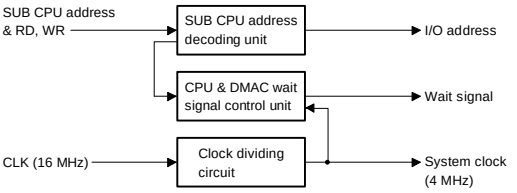

SUB CPU address & RD, WR
SUB CPU address decoding unit
I/O address
CPU & DMAC wait signal control unit
Wait signal
CLK (16 MHz)
Clock dividing circuit
System clock (4 MHz)

Fig. 5

(a) I/O address generation circuit
A total of 11 I/O addresses are generated by A0, A1, A4, A5 and RD and WR signals.

(b) CPU and DMAC wait signal control unit
Clocks into the CPU (Z-80), SUB CPU and its peripheral LSI, DMAC and CTC are operated respectively on 4 MHz.
While, the ADLC (MC68B54) (Advanced Data Link Control) is operated by the E (Enable clock) of 2 MHz according to restrictions in terms of the hardware of the LSI.
It is necessary to synchronize the timing of the write and read in the ADLC.
To control synchronization, timing, and input, the wait signal goes into the CPU for CPU access and into the DMAC for DMA access. This block is a circuit to generate such wait signal.

(c) Clock dividing circuit
This block divides the blocks according to the CLK supplied from outside to generate the clock for CPU, DMAC and CTC and the E and transmission clock rate (480 KBPS or 1 MBPS selectable) for the ADLC.

(3) Transmission control circuit

The transmission control circuit is divided into the modem unit, carrier detect unit, collision detect unit.

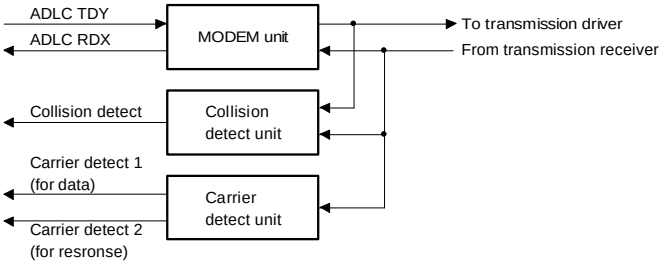


Fig. 6

(a) Modem circuit
The transmission data input from the ADLC are PE modulated (phase encoding modulation), the circuit to be output to the transmission driver and the reception data input from the transmission receiver are demodulated and produced at the ADLC.

(b) Collision detect circuit
The data transmitted from the home station is received and detects a collision on the transmission line by means of an exclusive OR gate.

(c) Carrier detect circuit
This circuit detects whether data is flowing on the transmission line. It consists of a circuit which immediately senses a no data status on the line. When data is not on the line the circuit functions to sense an elapse of the fixed time rate. The immediate sensing circuit is used for response testing and the delayed sensing circuit is used for data testing.
The fixed time rate is selectable according to the transmission speed as shown below via SRV-mode programming. Job #922.

Transmission speed	Delay time
1 MBPS	1.6m sec, 3.2m sec, 4.8m sec, 6.4m sec.
480 KBPS	3.2m sec, 6.4m sec, 9.6m sec, 12.8m sec.

3) Terminal Name and Description (MB62H149)

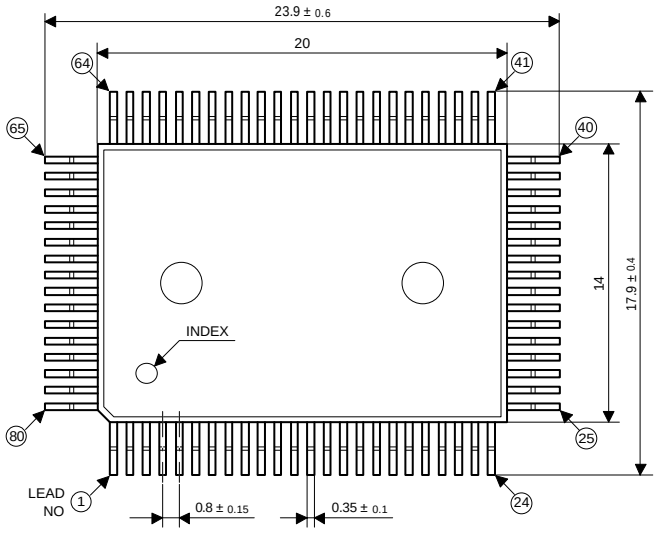


Fig. 7

Pin No.	Terminal name	Host/ Sub	In/ Out	Description
1	CLK	Sub	In	Clock in (16 MHz)
2	—	—	—	N.U.
3	$\overline{\text{IORQ}}$	Sub	In	I/O request
4	$\overline{\text{MREQ}}$	Sub	In	Memory request
5	$\overline{\text{RDS}}$	Sub	In	Read from sub
6	$\overline{\text{WRS}}$	Sub	In	Write from sub
7	$\overline{\text{INTS}}$	Sub	Out	Interrupt to sub
8	ϕ	Sub	Out	Clock out
9	TM0	Sub	In	Timer 0
10	TM1	Sub	Out	Timer 1
11	$\overline{\text{MRD}}$	Sub	Out	Memory read
12	VSS	—	—	GND
13	$\overline{\text{WAIT}}$	Sub	Out	Wait signal
14	A15	Sub	Out	Address bus for DMA
16	A9	Sub	Out	
17	A8	Sub	Out	
18	A5	Sub	In	
19	A4	Sub	In	
20	A1	Sub	In	
21	A0	Sub	In	
22	DAK01	Sub	In	DMA acknowledge 0+1
23	—	—	—	N.U.
24	$\overline{\text{MWR0}}$	Sub	Out	Memory write
25	D7	Sub	I/O	Data bus
26	D6	Sub	I/O	
27	D5	Sub	I/O	
28	D4	Sub	I/O	
29	D3	Sub	I/O	
30	D2	Sub	I/O	
31	D1	Sub	I/O	
32	D0	Sub	I/O	
33	VDD	—	—	+5V
34	—	—	—	N.U.
35	$\overline{\text{RES}}$	Host	In	Reset
36	$\overline{\text{IO/WR}}$	Sub	I/O	I/O write
37	$\overline{\text{IO/RD}}$	Sub	I/O	I/O read
38	AEN	Sub	In	Address enable from DMAC
39	AST	Sub	In	Address strobe from DMAC
40	TCS	Sub	In	Terminal count
41	DAK23	Sub	In	DMA acknowledge 2+3
42	$\overline{\text{DRQRS}}$	Sub	Out	DMA request read to sub
43	$\overline{\text{DRQWS}}$	Sub	Out	DMA request write to sub
44	$\overline{\text{RDH}}$	Host	In	Read from Host
45	$\overline{\text{WRH}}$	Host	In	write from Host
46	$\overline{\text{INTH}}$	Host	Out	Interrupt to host
47	$\overline{\text{DAK}}$	Host	In	DMA acknowledge from host
48	TCH	Host	In	Terminal count from host
49	$\overline{\text{DRQWH}}$	Host	Out	DMA request read to host
50	$\overline{\text{DRQWH}}$	Host	Out	DMA request write to host
51	$\overline{\text{CS}}$	Host	In	Chip select from host
52	VSS	—	—	GND
53	—	—	—	N.U.
54	DB0	Host	I/O	Data bus
55	DB1	Host	I/O	Data bus
56	DB2	Host	I/O	Data bus
57	DB3	Host	I/O	Data bus
58	DB4	Host	I/O	Data bus
59	DB5	Host	I/O	Data bus
60	DB6	Host	I/O	Data bus
61	DB7	Host	I/O	Data bus
62	AB0	Host	In	Address bus from host
63	—	—	—	N.U.
64	AB1	Host	In	Address bus from host
65	COL	Sub	In	Collision detect signal
66	RDI	Sub	In	Receive data from receiver
67	TDI	Sub	Out	Transmmit data to driver
68	$\overline{\text{RTS}}$	Sub	In	Request to send
69	RXC	Sub	Out	Receive clock to ADLC
70	RXD	Sub	Out	Receive data to ADLC
71	TXC	Sub	Out	Transmmit clock
72	TXD	Sub	In	Transmmit data
73	VDD	—	—	+5V
74	E	Sub	In	Enable clock to ADLC
75	$\overline{\text{IRQ}}$	Sub	In	Interrupt request from ADLC
76	$\overline{\text{LCS}}$	Sub	Out	Link controller chip select
77	—	—	—	N.U.
78	RS1	Sub	Out	Register select 1
79	RS0	Sub	Out	Register select 0
80	MSK	Sub	Out	Mask signal

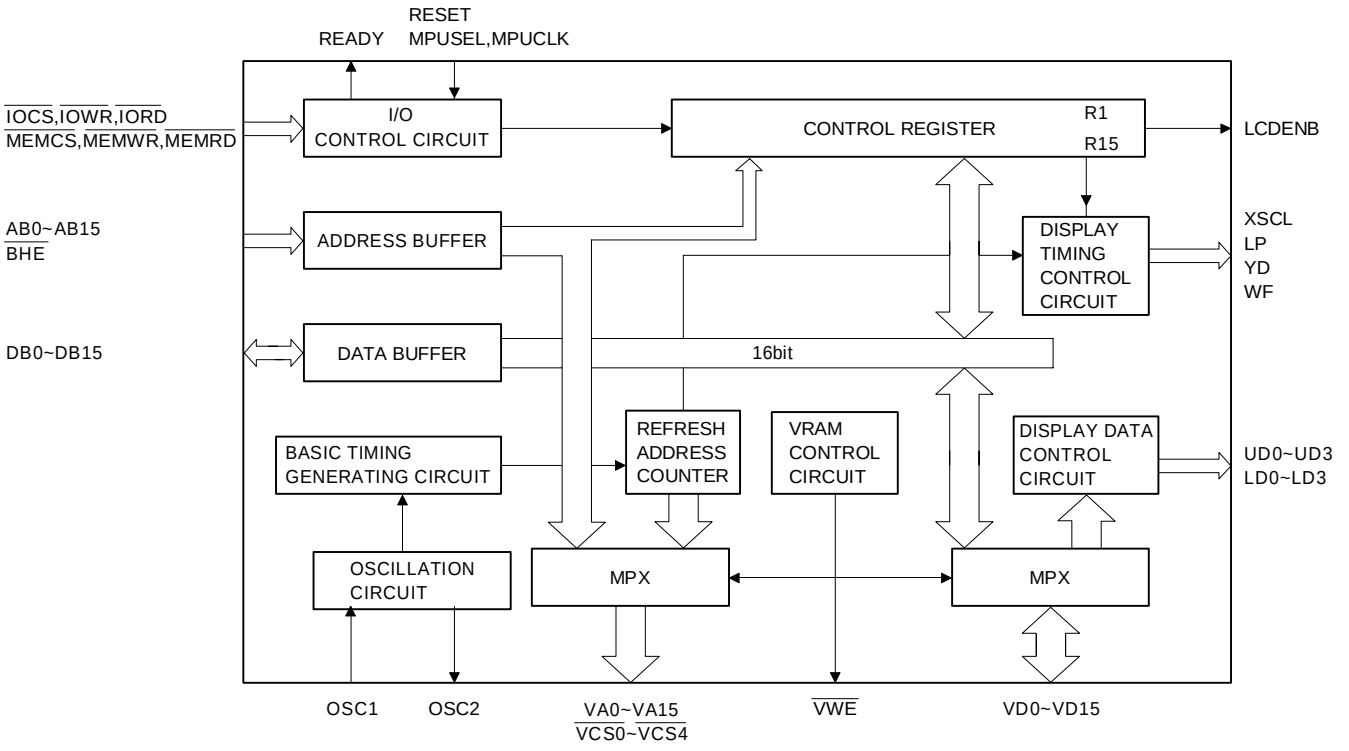
2-9. SED1351FOA/LB

The SED1351FOA/LB is a display controller that is used for the high-duty dot matrix type LCD for graphic display.
This unit can interface with an 8-bit or 16-bit MPU with the READY ($\overline{WAIT}$) input terminal. Access to the VRAM is performed by the cycle steal method so that distortion of the screen is minimal. Also, the unit incorporates all the addresses and the data control circuits necessary for cycle steal, requiring no external circuit. The chip select output terminal for VRAM allows direct connection of eight 64K SRAMs or two 256K SRAMs without having to use any external decoder circuit.
The VRAM is mapped on the MPU's memory space to make it possible to address all the display data directly from the MPU, thus providing efficient processing of display data including those of pictures.
The SED1351F$_{OA}$ has two display modes: the conventional ON/OFF binary display mode and the gradation display mode including ON/OFF and pseudo intermediate double tone. In the binary display mode, the maximum number of display dots is 524288 dpi and in the gradation display mode, it is 262144 dpi, when all the 64KB of memory of the VRAM.

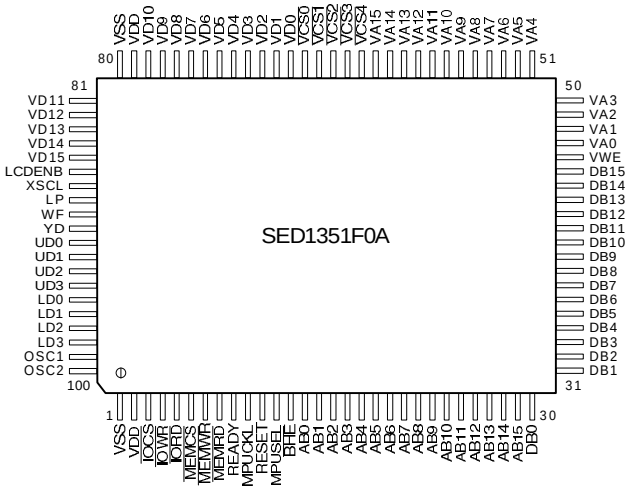
1) FEATURES:

- The unit can be controlled with an 8-bit or 16-bit MPU (Intel MPU).
- Can be interfaced with the MPU by the READY ($\overline{WAIT}$) signal.
- Access from MPU to VRAM is performed through the cycle steal method $\rightarrow$ No effect on the screen.
- VRAM
  Mapping ..... MPU memory space
  Capacity ..... 64 Kbytes (2^{16})
- LCD display mode
  Binary display mode (ON/OFF)
  Graduation display mode (ON/OFF and pseudo intermediate double tone)
- LCD panel
  Single screen drive panel (Transfer by 4 bits or 8 bits*)
  Double screen drive panel (4 bits $\times$ 2)
- Maximum number of characters in horizonal direction
  (256 characters)
  2048 dots (binary display mode)
  1024 dots (graduation display mode)
- Maximum number of vertical lines
  1024 lines (single screen drive)
  2048 lines (double screen drive)
- Divided screen/OR function (Either function is available when single screen drive is set)
  Divided screen ... The screen can be divided into two upper and lower sections.
  OR function ..... Two different data can ORed.
- Virtual display can be set.
- Smooth scroll in vertical direction.
- Built-in chip select output for VRAM.
- CMOS operation

2) Block diagram



3) Pin configuration


SED1351F0A
VSS VDD VD10 VD9 VD8 VD7 VD6 VD5 VD4 VD3 VD2 VD1 VD0 VCS0 VCS1 VCS2 VCS3 VCS4 VA15 VA14 VA13 VA12 VA11 VA10 VA9 VA8 VA7 VA6 VA5 VA4
80 51
81 50
VD11 VD12 VD13 VD14 VD15 LCDENB XSCL LP WF YD UD0 UD1 UD2 UD3 LD0 LD1 LD2 LD3 OSC1 OSC2
VA3 VA2 VA1 VA0 VWE DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
100 31
1 30
VSS VDD IOCS IOWR IORD MEMCS MEMWR MEMRD READY MPUCKL RESET MPUSEL BHE AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15 DB0

4) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	VSS	GND	—	GND
2	VDD	VCC	—	+5V
3	$\overline{\text{IOCS}}$	$\overline{\text{LCDC}}$	In	Chip select signal for control register
4	$\overline{\text{IOWR}}$	$\overline{\text{WR}}$	In	Write strobe signal for control register
5	$\overline{\text{IORD}}$	$\overline{\text{RD}}$	In	Read strobe signal for control register
6	$\overline{\text{MEMCS}}$	$\overline{\text{RASV}}$	In	VRAM chip select signal
7	$\overline{\text{MEMWR}}$	$\overline{\text{WR}}$	In	VRAM write strobe signal
8	$\overline{\text{MEMRD}}$	$\overline{\text{RD}}$	In	VRAM read strobe signal
9	READY	LCDWT	Out	Ready signal
10	MPUCLK	#	In	Clock signal
11	RESET	$\overline{\text{RESET}}$	In	Reset signal
12	MPUSEL	GND	In	GND
13	$\overline{\text{BHE}}$	VCC	In	+5V
14	AB0	A0	In	Address bus
15	AB1	A1	In	Address bus
16	AB2	A2	In	Address bus
17	AB3	A3	In	Address bus
18	AB4	A4	In	Address bus
19	AB5	A5	In	Address bus
20	AB6	A6	In	Address bus
21	AB7	A7	In	Address bus
22	AB8	A8	In	Address bus
23	AB9	A9	In	Address bus
24	AB10	A10	In	Address bus
25	AB11	A11	In	Address bus
26	AB12	A12	In	Address bus
27	AB13	A13	In	Address bus
28	AB14	A14	In	Address bus
29	AB15	A15	In	Address bus
30	DB0	D0	In/Out	Data bus
31	DB1	D1	In/Out	Data bus
32	DB2	D2	In/Out	Data bus
33	DB3	D3	In/Out	Data bus
34	DB4	D4	In/Out	Data bus
35	DB5	D5	In/Out	Data bus
36	DB6	D6	In/Out	Data bus
37	DB7	D7	In/Out	Data bus
38	DB8	GND	—	GND
39	DB9	GND	—	GND
40	DB10	GND	—	GND
41	DB11	GND	—	GND
42	DB12	GND	—	GND
43	DB13	GND	—	GND
44	DB14	GND	—	GND
45	DB15	GND	—	GND
46	$\overline{\text{VWE}}$	$\overline{\text{VWE}}$	Out	VRAM write strobe signal
47	VA0	VA0	Out	VRAM address bus
48	VA1	VA1	Out	VRAM address bus
49	VA2	VA2	Out	VRAM address bus
50	VA3	VA3	Out	VRAM address bus
51	VA4	VA4	Out	VRAM address bus
52	VA5	VA5	Out	VRAM address bus
53	VA6	VA6	Out	VRAM address bus
54	VA7	VA7	Out	VRAM address bus
55	VA8	VA8	Out	VRAM address bus
56	VA9	VA9	Out	VRAM address bus
57	VA10	VA10	Out	VRAM address bus
58	VA11	VA11	Out	VRAM address bus
59	VA12	VA12	Out	VRAM address bus
60	VA13	VA13	Out	VRAM address bus
61	VA14	VA14	Out	VRAM address bus
62	VA15	NC	—	NC
63	$\overline{\text{VCS4}}$	NC	—	NC
64	$\overline{\text{VCS3}}$	NC	—	NC
65	$\overline{\text{VCS2}}$	NC	—	NC
66	$\overline{\text{VCS1}}$	$\overline{\text{VCS1}}$	Out	VRAM chip select signal
67	$\overline{\text{VCS0}}$	$\overline{\text{VCS0}}$	Out	VRAM chip select signal
68	VD0	VD0	In/Out	VRAM data bus
69	VD1	VD1	In/Out	VRAM data bus
70	VD2	VD2	In/Out	VRAM data bus
71	VD3	VD3	In/Out	VRAM data bus
72	VD4	VD4	In/Out	VRAM data bus
73	VD5	VD5	In/Out	VRAM data bus
74	VD6	VD6	In/Out	VRAM data bus
75	VD7	VD7	In/Out	VRAM data bus
76	VD8	VCC	—	+5V
77	VD9	VCC	—	+5V
78	VD10	VCC	—	+5V
79	VDD	VCC	—	+5V
80	VSS	VCC	—	+5V
81	VD11	VCC	—	+5V
82	VD12	VCC	—	+5V
83	VD13	VCC	—	+5V
84	VD14	VCC	—	+5V
85	VD15	VCC	—	+5V
86	LCDENB	LCDENB	Out	LCD control signal
87	XSCL	XSCL	Out	Clock for display data transmission
88	LP	LP	Out	Display data latch pulse signal
89	WF	WF	Out	Frame signal (Liquid crystal alternating current signal)
90	YD	YD	Out	Scanning line start signal
91	UD0	UD0	Out	Screen display data
92	UD1	UD1	Out	Screen display data
93	UD2	UD2	Out	Screen display data
94	UD3	UD3	Out	Screen display data
95	LD0	NC	—	NC
96	LD1	NC	—	NC
97	LD2	NC	—	NC
98	LD3	NC	—	NC
99	OSC1	OSC1	In	System clock
100	OSC2	OSC2	Out	System clock

2-10. CKDC7 (HD404728A91FS)

1) General description

The CKDC7 is a 4-bit microcomputer developed for the ER-A750 and provides functions to control the real-time clock, keys, and displays. The basic functions of the CKDC7 are shown below.

Keys: The CKDC7 is capable of controlling a maximum of 256 momentary keys. (Sharp 2-key rollover control)
Simultaneous scanning of key and switch
(When a key is scanned, the state of a mode and clerk switch is also buffered. The host can scan the state of switch together with the key entry data at the same time the key is scanned.)

Switches: Mode switch with 14 positions maximum
8-bit clerk (cashier) switch
2-bit feed switch
1-bit receipt on/off switch
1-bit option switch
4-bit general-purpose switch (1-bit is used for keyboard select)

Displays: 16-column dot display
12-column 7-segment display (column digit selectable)
All column blink controlled for the dot and 7-segment display decimal point and indicators
Programmable patterns for 7-segment display:
Four patterns
Internal driver for 7-segment display

Buzzer: Single tone control

Clock: Year, month, day of month, day of week, hour, minute

Alarm: Hour, minute

Interrupt request (event control):
Detection of key input, switch position change, alarm issue, and counter overflow

2) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	SB	SB	Out	Segment B
2	SC	SC	Out	Segment C
3	SD	SD	Out	Segment D
4	SE	SE	Out	Segment E
5	SF	SF	Out	Segment F
6	SG	SG	Out	Segment G
7	P4	COM/AP	Out	
8	P0	NC	—	NC
9	P1	NC	—	NC
10	P2	DP	Out	Decimal point
11	P3	ID	Out	Indicator
12	$\overline{\text{MODR}}$	VCC	—	+5V
13	$\overline{\text{CFSR}}$	$\overline{\text{CFSR}}$	In	Clerk key, Feed key, Switch return signal
14	KEX0	KEX0	Out	Key exchange signal
15	KEX1	KEX1	Out	Key exchange signal
16	RQ	GND	—	GND
17	SKR0	VCC	—	+5V
18	ST0	ST0	Out	Key strobe signal
19	ST1	ST1	Out	Key strobe signal
20	ST2	ST2	Out	Key strobe signal
21	ST3	ST3	Out	Key strobe signal
22	$\overline{\text{POFF}}$	$\overline{\text{POFF}}$	In	Power off signal
23	$\overline{\text{STOP}}$	$\overline{\text{STOP}}$	In	STOP signal
24	$\overline{\text{DDIG}}$	VCC	—	+5V
25	$\overline{\text{DCS}}$	NC	—	NC
26	VCC	VCC	—	+5V
27	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$	In	Clock signal
28	HTS	HTS	In	Key data from host
29	STH	STH	Out	Key data to host
30	SDISP	GND	—	GND
31	BUZZ	BUZZ	Out	Buzzer
32	$\overline{\text{DSCK}}$	NC	—	NC
33	$\overline{\text{SRES}}$	$\overline{\text{RESET}}$	Out	Reset signal
34	DS0	NC	—	NC
35	$\overline{\text{SHEN}}$	$\overline{\text{SHEN}}$	Out	Shift enable signal
36	$\overline{\text{IRQ}}$	$\overline{\text{IRQ}}$	Out	Key request signal
37	KR0	$\overline{\text{KR0}}$	In	Key return signal
38	KR1	$\overline{\text{KR1}}$	In	Key return signal
39	KR2	$\overline{\text{KR2}}$	In	Key return signal
40	KR3	$\overline{\text{KR3}}$	In	Key return signal
41	RESET	CKDCR	In	CKDC reset signal
42	OSC2	OSC2	—	Clock
43	OSC1	OSC1	—	Clock
44	GND	GND	—	GND
45	CL1	CL1	—	Time clock
46	CL2	CL2	—	Time clock
47	TEST	VCC	—	+5V
48	G0	G0	Out	Display digit signal
49	G1	G1	Out	Display digit signal
50	G2	G2	Out	Display digit signal
51	G3	G3	Out	Display digit signal
52	G4	G4	Out	Display digit signal
53	G5	G5	Out	Display digit signal
54	G6	G6	Out	Display digit signal
55	G7	G7	Out	Display digit signal
56	G8	G8	Out	Display digit signal
57	G9	G9	Out	Display digit signal
58	G10	G10	Out	Display digit signal
59	G11	G11	Out	Display digit signal
60	PO0	NC		NC
61	PO1	NC		NC
62	PO2	NC	—	NC
63	PO3	NC	—	NC
64	SA	SA	—	Segment A

3. Address map

3-1. Total memory space

The address map of the total memory space is shown below. As you can see, the memory space is divided into the following 5 blocks:

- 0page area (including the I/O area)
- VRAM
- RAM
- ROM
- Extended I/O area

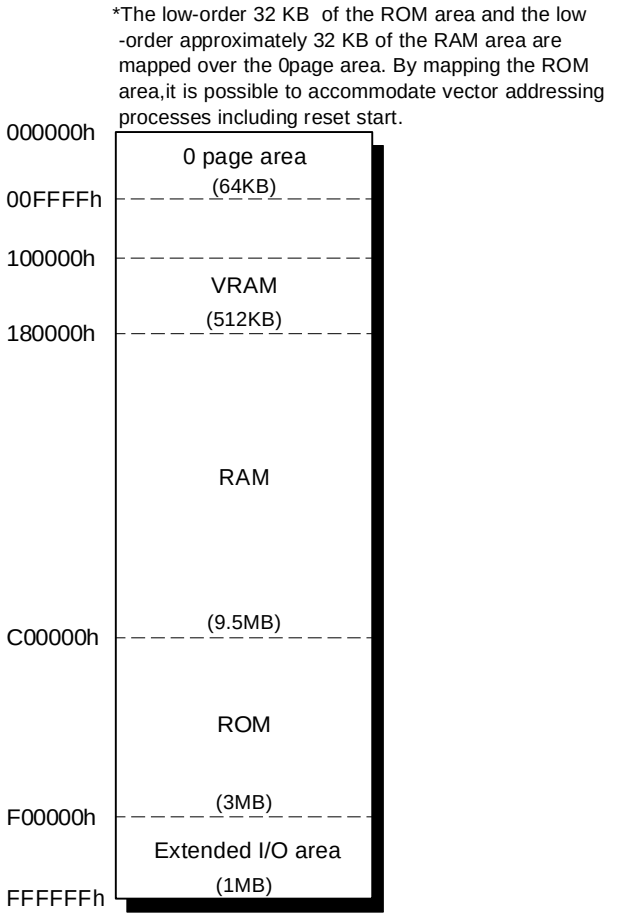

*The low-order 32 KB of the ROM area and the low -order approximately 32 KB of the RAM area are mapped over the 0page area. By mapping the ROM area,it is possible to accommodate vector addressing processes including reset start.
000000h
0 page area
(64KB)
00FFFFh
100000h
VRAM
(512KB)
180000h
RAM
(9.5MB)
C00000h
ROM
(3MB)
F00000h
Extended I/O area
(1MB)
FFFFFFh
*The extended I/O area is a space for I/O devices which are to be addressed in spaces other than the 0page area.In the MPCA7,the addresses from FFFF00h to FFFFFFh are used for the SSP's addd-ressing register.

Fig. 2

3-2. 0page area

The 0page area consists of four spaces: the ROM mapped area, RAM mapped area, internal and external I/O areas.

The ROM and RAM mapped spaces have been devised for the following purposes:

① Simplifying the procedure for booting the IPL program

② Separating the static RAM access from file space.

③ Achieving high-speed accessing, and accessing by abbreviated instructions.

∗ In the ER-A750, the low-order 32 KB of the RASP space (180000h ~ 1FFFFFh) is mapped (With the MPCA7's internal registers RASPE=1 and RASEL=0, the address line MA15 should be used.)

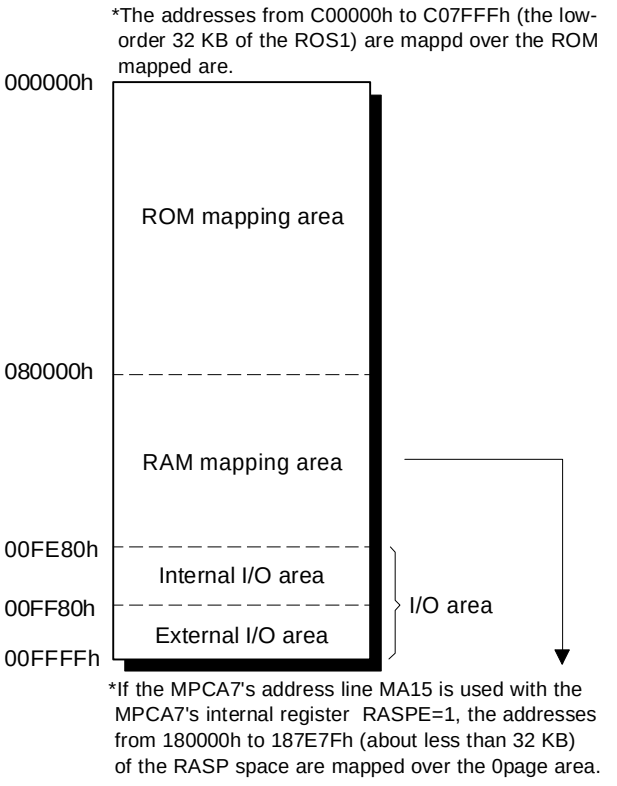

*The addresses from C00000h to C07FFFh (the low-order 32 KB of the ROS1) are mappd over the ROM mapped are.
000000h
ROM mapping area
080000h
RAM mapping area
00FE80h
Internal I/O area
00FF80h
External I/O area
00FFFFh
I/O area
*If the MPCA7's address line MA15 is used with the MPCA7's internal register RASPE=1, the addresses from 180000h to 187E7Fh (about less than 32 KB) of the RASP space are mapped over the 0page area.

Fig. 3

3-3. I/O areas

The addresses from 00FE80h to 00FF7Fh are called the internal I/O area, while those from 00FF80h to 00FFFFh the external I/O area.

The internal I/O area is a space where the control registers and built-in ports inside the CPU are addressed.

The external I/O area is a space where the peripheral devices outside the CPU or devices on an optional card are addressed.

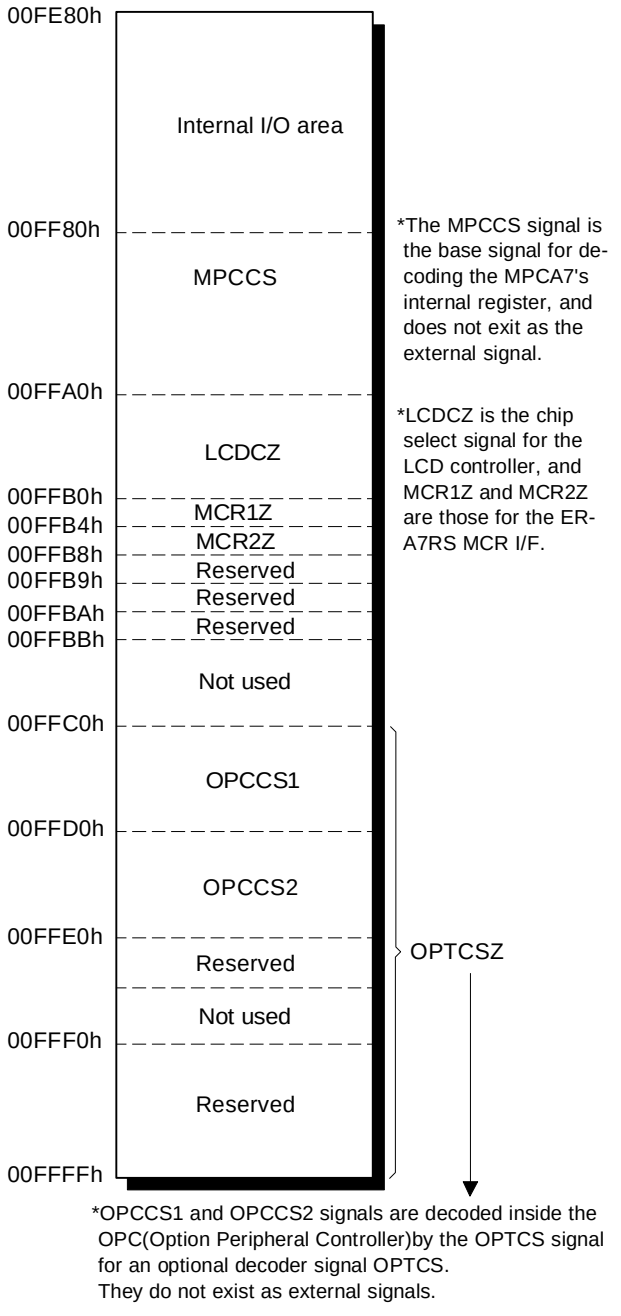


Fig. 4

3-4. ROM space

Fig.5 shows the ROM space. The ER-A750 uses 1MB of NOR-type flash memory instead of conventional ROM, so that the ROS1 and ROS2 from the MPCA7 are ORed and input into the chip enable of the flash memory.

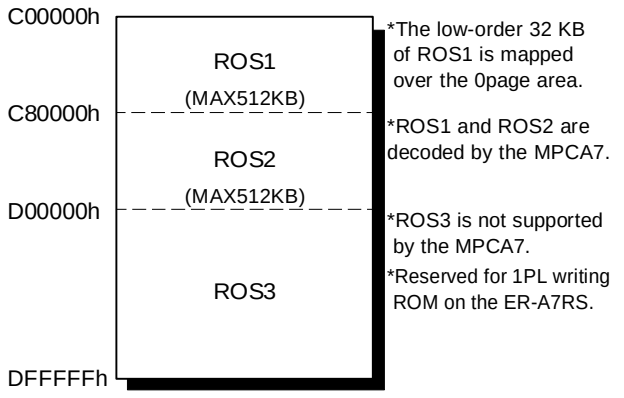


Fig. 5

3-5. VRAM & RAM space

The VRAM is the display memory of the LCD. Correspondence of the memory address and the display content is described Section 5 Display.

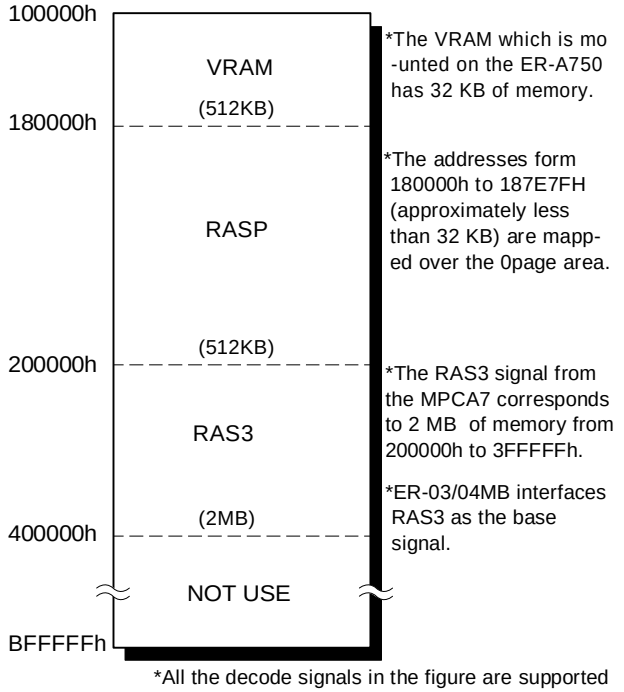

100000h
VRAM
(512KB)
180000h
RASP
(512KB)
200000h
RAS3
(2MB)
400000h
NOT USE
BFFFFFh
*The VRAM which is mo -unted on the ER-A750 has 32 KB of memory.
*The addresses form 180000h to 187E7FH (approximately less than 32 KB) are mapped over the 0page area.
*The RAS3 signal from the MPCA7 corresponds to 2 MB of memory from 200000h to 3FFFFFh.
*ER-03/04MB interfaces RAS3 as the base signal.
*All the decode signals in the figure are supported by the MPCA7.

Fig. 6

3-6. Extended I/O area

The addresses from F00000h to FFFFFFh are called an extended I/O area. The ER-A750 uses the following addresses as the break address register (BAR) for SSP.

- FFFF00h ~ FFFFFFh

4. LCD display

The main display is a 320 × 240 dot liquid crystal display. The display controller is capable of performing cycle steal actions (discussed later), thus achieving high-speed display.

4-1. Block diagram

Here is the block diagram of the LCD and its allied components.

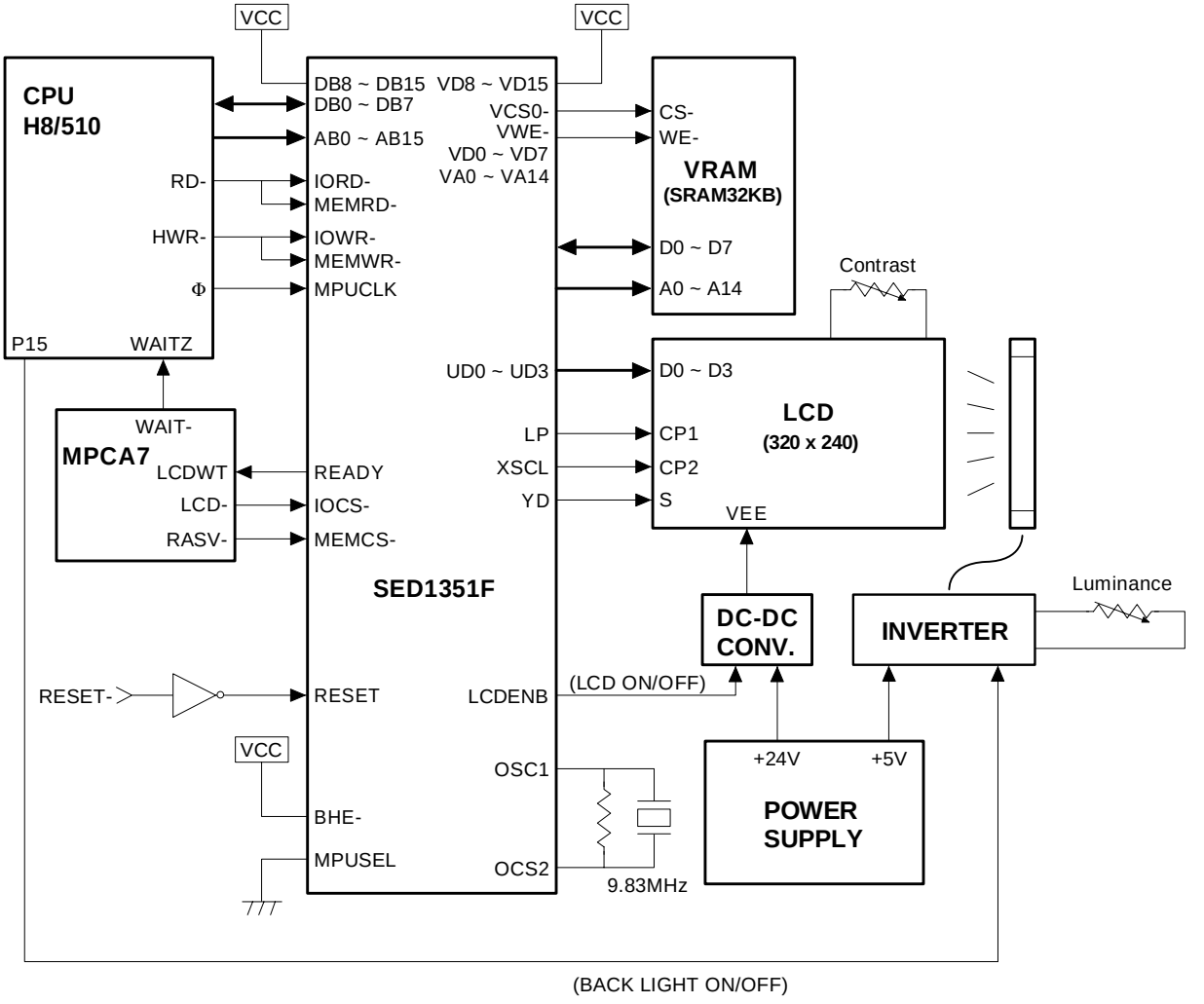


Fig. 7

4-2. LCD panel

The LCD panel is the model LM320153 dot-matrix liquid crystal unit, which is a blue-mode transmission type with a CCFT back light.

The resolution is 320 × 240 dots, with each dot size being 0.33 × 0.33.

4-3. Display controller

The display controller is the Epson SED1351F0A. VRAM is located on the address space of the CPU and it is possible to write and read data freely to and from the CPU. Access to VRAM is performed in the cycle steal method, so that data can be written and read without disturbing the display screen while the screen is scanned. (While the screen is scanned, access to VRAM is inhibited; Instead, VRAM is generally accessed at the fly-back time.)

VRAM uses 32 KB of SRAM.

4-4. LCD ON controller

The LCD display is turned ON and OFF by controlling the LCD power supply VEE through the LCDENB terminal of the SED1351.

The LCDENB is in the "L" state after resetting. Electric power is supplied from the VEE to the LCD by setting the LCDE bit inside the R1 register of the SED1351 to "H". This makes it possible to turn ON the LCD display.

4-5. Back light control

The back light is turned on and off through the port P15 of the CPU. The initial value is "L" in which the back light is OFF. Writing "H" in the P15 turns the back light on.

4-6. Luminance and contrast adjustment

- Luminance: Luminance is adjusted with an inverter which has dimming function.
- Contrast: Contrast is adjusted by controlling the contrast adjustment voltage (V0) of the LM320153.

5. Customer display

The customer display uses the same vacuum fluorescent tube (FIP7B13) as the ER-A8DP has. The display is turned on and off by the CKDC7.

6. Pseudo SRAM

Here is an explanation for pseudo SRAM interfaces.

6-1. CPU interface

The figure below shows a typical pseudo SRAM interface in the ER-31X system.

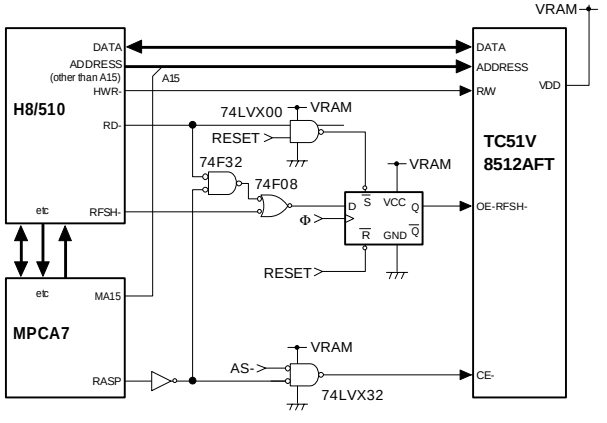


Fig. 8

6-2. Pseudo SRAM address

To use the decoding signal RASP for the pseudo SRAM, RASPE, or the RASP enabling bit for the MPCA7, must be first enabled. When RASPE is enabled, the pseudo SRAM is decoded by the RASP signal as follows:

① 180000h ~ 1FFFFFh

② 008000h ~ 00FE7Fh (same as 180000h ~ 187E7Fh)

In 2, the 0page mapping function of the MPCA7 is used. Approximately 30 KB from the beginning of the addresses in the pseudo SRAM can be also accessed from the 0page space.

7. NOR-type flash memory

Here is the explanation for the interface of NOR-type flash memory. The device is Sharp's LH28F800SU flash memory which consists of 512 K words × 16 or 1 MB × 8, with 16 blocks of 64 KB.

In addition, the LH28F800SU is the second-generation device, which has a number of functional blocks including page buffer, command queue, and block status register. Taking advantage of these functions will improve the performance, especially in writing data.

7-1. CPU interface

The figure below shows a typical interface for the LH28F800SU of the ER-A750 system.

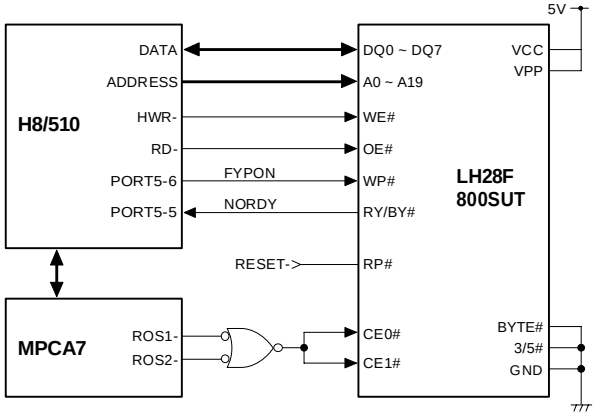


Fig. 9

7-2. Device control

After resetting, the device automatically enters the array read mode and perform the same action as the usual ROM, thus requiring no special consideration when reading data.

Data can be written at high speed by using the page buffer.

8. SSP control

The ER-A750 uses flash memory in the place of EPROM, so it is possible to rewrite the contents of the flash memory in changing the program. However, since the existing gate array MPCA7 is used, it is also possible to use the conventional SSP.

8-1. Operation

Like the MPCA6, the MPCA7 adopts the break address register comparison method for detecting addresses. The operation of this method is briefly explained below.

The gate array always compares the break address register (ABR) built in the gate array, with the address bus to monitor the address bus.

If both agree, the gate array outputs the NMI signal to the CPU, which in turn shifts from normal handling to exception handling.

In both the MPCA6 and the MPCA7, SSP is achieved by the above operation.

The setting of the break address register (BAR) is directly written in the addresses from FFFF00h to FFFFFFh.

9. Interrupt control

There are roughly two types of interrupts:

- Internal interrupts: Controlled inside the CPU
- External interrupts: Input into the CPU from outside

9-1. Internal interrupts

Device interrupts built in the CPU are used for the following applications:

Table 8

Event factor		Application
SC11		Interrupt source as IR channel
SC12		Not used (SC1 is used for CKDC interface.)
FRT1	(ICI) (OCRA) (OCRB) (OVF)	INTMCR ~ MCR interrupt (to FT11 terminal)
FRT2	(ICI) (OCRA) (OCRB) (OVF)	Standard SHEN event (for CKDC) Simple IRC timer event RS232 timer event System timer (53 ms)
TMR	(CMA) (CMB) (OVF)	
WDT	(OVF)	Drawer open timer
A/D		Not used
NMI		SSP request

9-2. External interrupts

The following types of external interrupts are available:

- $\overline{\text{NMI}}$ (SSP)
- $\overline{\text{IRQ0}}$ (Standard I/O interrupt)
- $\overline{\text{IRQ1}}$ (RS232 interrupt)
- $\overline{\text{IRQ2}}$ (Used as SCk terminal)
- $\overline{\text{IRQ3}}$ (Used as SCK terminal)

9-2-1. IRQ0 layout

The interrupt factors for a total of 16 standard I/Os are ORed inside the MPCA7 and input into the CPU as IRQ0. Each interrupt factor can be read by the internal register of the MPCA7.

Table 9

<IRQ0 component bits – 1>

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00FF80h	$\overline{\text{POFF}}$ (S17)	$\overline{\text{EXINT3}}$ (S16)	$\overline{\text{EXINT2}}$ (S15)	SI4	SI3	SI2	SI1	$\overline{\text{EXINT1}}$ (S10)

BIT7: $\overline{\text{POFF}}$ (SI7)
Power failure detection signal input and software interrupt 7 OR input

BIT6: $\overline{\text{EXINT3}}$ (SI6)
Optional external interrupt signal and software interrupt 6 OR input

BIT5: $\overline{\text{EXINT2}}$ (SI5)
Optional external interrupt signal and software interrupt 5 OR input

BIT4 ~ 1: SI4 ~ SI1
Software interrupt

BIT0: $\overline{\text{EXINT0}}$ (S10)

Table 10

<IRQ0 component bits – 2>

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00FF81h	—	$\overline{\text{EXINT0}}$	$\overline{\text{KRQ1}}$	$\overline{\text{SHEN1}}$ *	$\overline{\text{SHEN1}}$	—	—	—

*: Edge interrupt

BIT7: Not used

BIT6: $\overline{\text{EXINT0}}$
Optional external interrupt signal

BIT5-3: $\overline{\text{KRQ1}}$, $\overline{\text{SHEN1}}$
Event request signal for CKDC interface channel 1

9-2-2. IRQ1 layout

The IRQ1 is an external interrupt terminal for an external optional RS232, and input into the CPU through an optional slot bus.

9-2-3. IRQ2 layout

The IRQ2 terminal is used as the shift lock terminal (SCK1) for IR interface.

10. WAIT control

The weight control function built in the MPCA7 is used to provide an interface with low-speed devices.

10-1. Block diagram

The block diagram of the weight control function is shown in Figure 10.

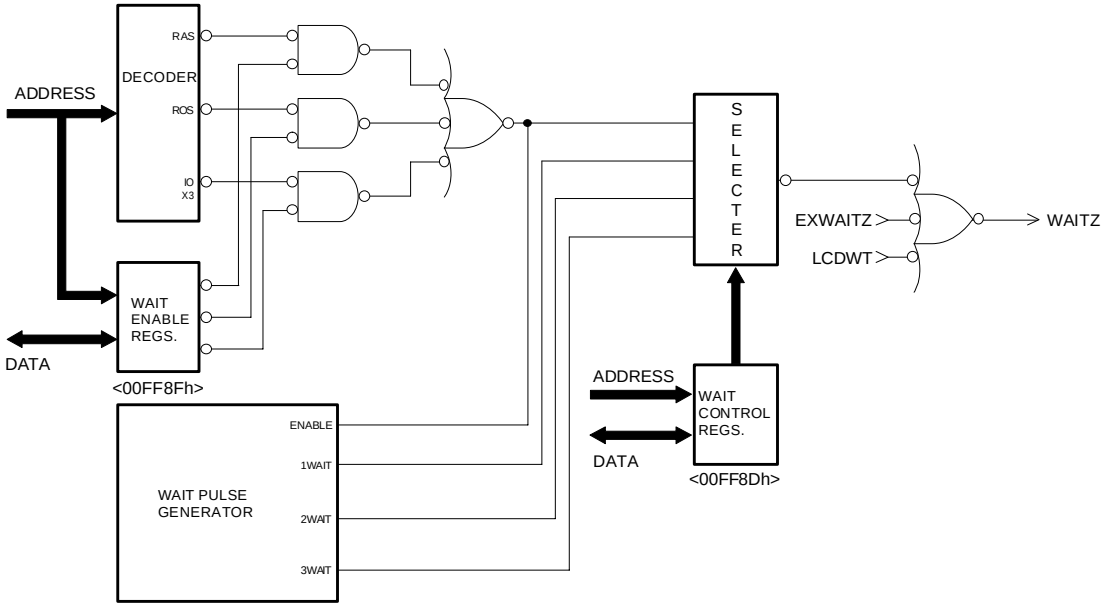


Fig. 10

In the figure, the decoder, wait enabling register, AND-OR sections are the same as those in the MPCA5 or 6, but other components are newly incorporated in the MPCA7.

EXWAITZ and LCDWT are external weight signals which are to be ORed inside the CPU and output to the WAITZ. The EXWAITZ is a general-purpose wait request terminal, and LCDWT is the wait request signal from the LCD controller.

11. CKDC7

The ER-A750 performs the following controls, using CKDC7.

- Keyboard
- Customer display
- Clock
- Buzzer
- System reset

11-1 Interface

CKDC7 is connected through the MPCA7.

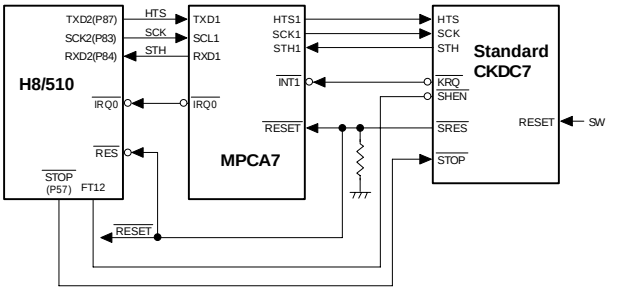
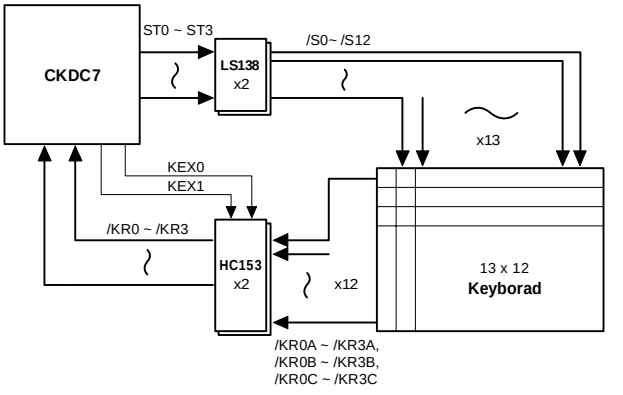


Fig. 11

12. Keyboard

The ER-A750 uses the 13x12 keyboard. The keyboard is controlled through the CKDC7.

12-1. Interface



13. RAM expansion bus

As expansion RAM boards, the conventional ER-03MB and 04MB are used.

13-1. Interface

The ER-03/04 have been originally designed for use in the ER-A850. Therefore, when using the RAM expansion bus of the same construction for the ER-A750, the two following points on the interface need to be considered.

① Output address change

② Decode base signal change

Here is the explanation for the above two points:

① **Output address change**

The ER-A750 uses the expansion RAM board at the RAS3 area and its high-order IMB space (200000h ~ 3FFFFFh).

Basically, the ER-03MB is supposed to be used in the area from 300000h ~ 7FFFFFh; the ER-04MB in the area from 700000h ~ 8FFFFFh. Therefore, it is necessary to convert the addresses as shown below.

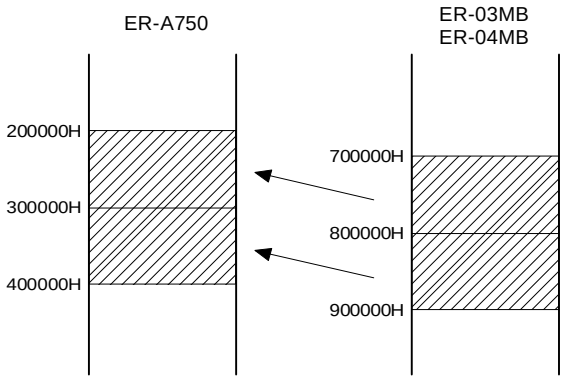


Fig. 12

Table 16

<Address conversion table>

ER-A750				
Address	A23	A22	A21	A20
2XXXXXh	0	0	1	0
3XXXXXh	0	0	1	1
4XXXXXh	0	1	0	0
5XXXXXh	0	1	0	1

↓

ER-03/04MB				
Address	RA23	RA22	RA21	RA20
7XXXXXh	0	1	1	1
8XXXXXh	1	0	0	0
9XXXXXh	1	0	0	1
AXXXXXh	1	0	1	0

In the tables, the address 400000h and after at the side of the ER-A750 are not used by the ER-03MB or ER-04MB, but is kept considering the commercialization of 4 Mb of expansion RAM in future.

The ER-03MB and ER-04MB use RA21 and RA20, respectively, because they do not have RA23 or RA22.

The address conversion circuit of RA21 and RA20 is shown below.

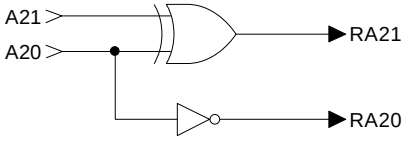


Fig. 13

② **Decode base signal change**

As decode signals, $\overline{\text{RAS3E}}$ and $\overline{\text{RAS30}}$ signals are generated for even and odd addresses, respectively, based on the RAS3 signal (200000h ~ 3FFFFFh). To allocate even and odd addresses, the address line A0 is used.

13-2. Terminal table

The terminal table of the RAM connector is shown below.

Table 17

<Expansion RAM connector terminal table>

Signal name	Pin No.	Pin No.	Signal name
GND	1	2	GND
GND	3	4	GND
RA21	5	6	RA20
PSX (Open)	7	8	$\overline{\text{PRAS30}}$
+5V	9	10	+5V
VCKDC	11	12	VCKDC
VRAM	13	14	VRAM
A16	15	16	A15
A14	17	18	$\overline{\text{WR}}$
A12	19	20	A13
A7	21	22	A8
A6	23	24	A9
A5	25	26	A11
A4	27	28	$\overline{\text{PSREF}}$
A3	29	30	A10
A2	31	32	A17
A1	33	34	A19
A0	35	36	$\overline{\text{PRAS3E}}$
A18	37	38	D7
D0	39	40	D6
D1	41	42	D5
D2	43	44	D4
$\overline{\text{RESET}}$	45	46	D3
GND	47	48	GND
GND	49	50	GND

✳ The signals in ( ) are not used.

14. I/O expansion bus specifications

The table below shows the standard bus for expanding optional devices

Table 18

Signal name	Pin No.	Pin No.	Signal name
GND	1	41	GND
GND	2	42	GND
$\overline{\text{RDO}}$	3	43	$\overline{\text{RD}}$
$\overline{\text{WRO}}$	4	44	$\overline{\text{EXWAIT}}$
+5V	5	45	$\overline{\text{BREQ}}$
+5V	6	46	$\overline{\text{BACK}}$
A23	7	47	$\overline{\text{TRQ2}}$
A22	8	48	$\overline{\text{TRQ1}}$
A21	9	49	$\overline{\text{EXINT1}}$
A20	10	50	$\overline{\text{EXINT0}}$
A19	11	51	N.C.
A18	12	52	$\overline{\text{IRQ1}}$
A17	13	53	$\overline{\text{RFSH}}$
A16	14	54	$\overline{\text{IPLON0}}$
A15	15	55	D7
A14	16	56	D6
A13	17	57	D5
A12	18	58	D4
A11	19	59	D3
A10	20	60	D2
A9	21	61	D1
A8	22	62	D0
A7	23	63	$\overline{\text{POFF}}$
A6	24	64	VCKDC
A5	25	65	+12V
A4	26	66	A3
← +24V	27	67	+24V
← +24V	28	68	+24V
A1	29	69	A2
A0	30	70	$\overline{\text{RES}}$
$\overline{\text{RESET}}$	31	71	$\overline{\text{AS}}$
$\overline{\text{OPTCS}}$	32	72	$\overline{\text{WR}}$
SYNC	33	73	
MCRRDY1	34	74	
MCRRDY2	35	75	
$\overline{\text{MCR1}}$	36	76	
$\overline{\text{MCR2}}$	37	77	–12V
	38	78	
GND	39	79	GND
GND	40	80	GND

15. Reset sequence

The reset sequence block diagram is shown below. Note that $\overline{\text{RESET}}$ signal (system reset) and $\overline{\text{CKDCR}}$ signal (CKDC reset) are different from each other.

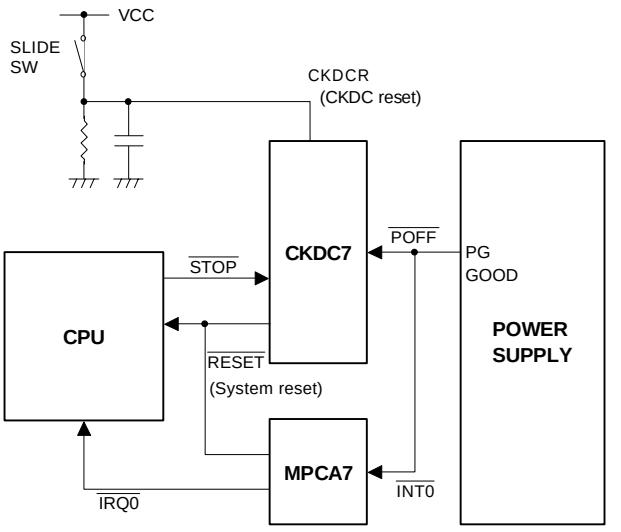


Fig. 14

15-1. Power ON/OFF

The flow of signal processing at the time of the power supply turning On/Off is as follows:

Table 19

<Power OFF>

	Power supply	MPCA6	CPU	CKDC7
1	$\overline{\text{POFF}} \rightarrow$ L			
2		$\overline{\text{IRQ0}} \rightarrow$ L		
3			$\overline{\text{STOP}} \rightarrow$ L	
4				$\overline{\text{RESET}} \rightarrow$ L (System reset)

Table 20

<Power ON>

	Power supply	MPCA6	CPU	CKDC7
1	$\overline{\text{POFF}} \rightarrow$ H			
2				$\overline{\text{RESET}} \rightarrow$ H (System reset)

The table below shows the timing chart.

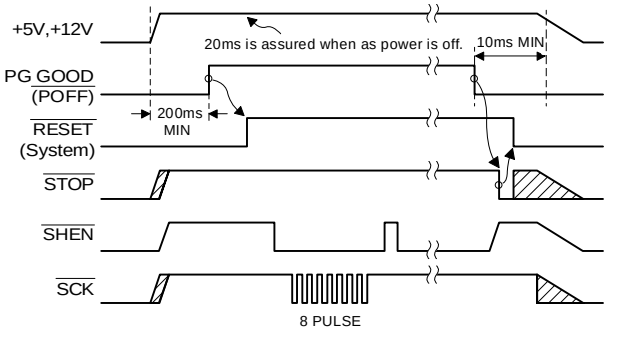


Fig. 15

15-2. MRS, SRV reset

The ER-A750 does not have the mode switch. The procedure for resetting MRS, SRV is different from that of conventional cash registers.

in the ER-A750, MRS, SRV resetting is selected and executed by the key which has bee depressed when the CKDC reset is released to start the system.

(In the case of MRS, security is added by a key operation equivalent to a pass word.)

Procedure

① POWER OFF

② Slide CKDC reset switch to reset position (slide switch)

③ POWER ON

④ Slide CKDC reset switch to normal position.

At this time,

- if no key is pressed, go to step ⑤
- if a specified key is pressed, go to step ⑥.

⑤ Perform program reset (SRV reset).

⑥ The machine waits for secret key input. Enter 4 kinds of secret keys before master resetting (secret key positions are fixed). Which type of master reset should be performed at this time (MRS1 or MRS2) is determined by the key which was pressed in step ④.
If the secret key input is wrong, reset the program. (The secret key input is like a pass word, to prevent the user from master resetting inadvertently.)

Flow chart

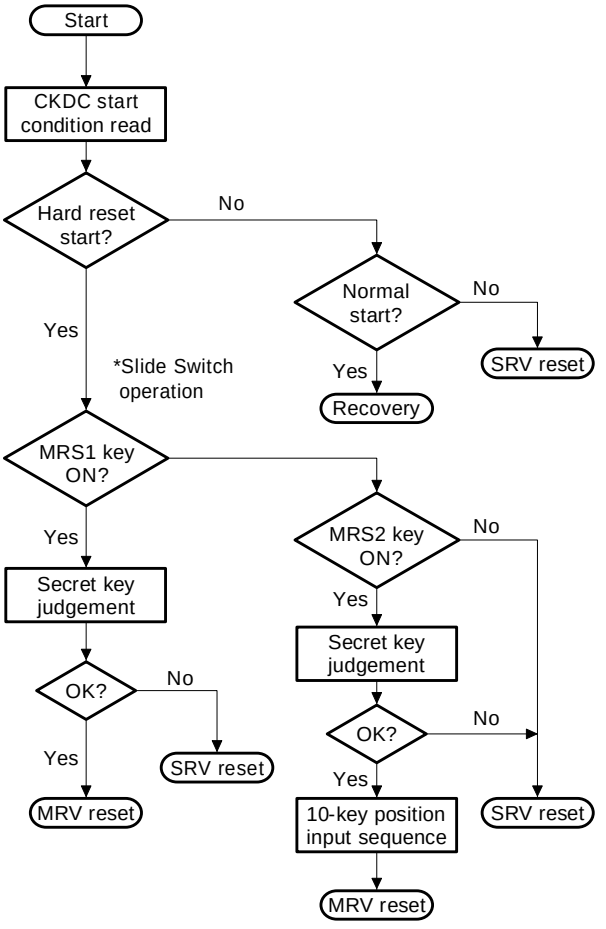


Fig. 16

16. Drawer

The ER-A750 can use up to 2 optional external drawers.

16-1. Drawer solenoid drive

P34 ~ P37 inside the CPU are allocated for the port output of the drawer solenoid drive.

Table 22

Built-in port	Signal name	Remarks
P34	$\overline{DR0}$	Drawer 1 (optional drawer)
P35	$\overline{DR1}$	Drawer 2 (optional drawer)
P36	$\overline{DR2}$	Reserved
P37	$\overline{DR3}$	Reserved

One port corresponds to one drawer. Theoretically, it is possible to drive multiple drawers at the same time, but this processing must be inhibited softwarewisely because of power supply capacity and driver hardware factors. If a power failure is detected, the drawer solenoid drive must be stopped as soon as possible.

✳ The drawer solenoid drive time must controlled in the range of 40 ms to 50 ms by the timer.

16-2. Drawer open/close sense

The drawer open/close sense signal is input into the built-in port of the CPU. the sense signal of an optional drawer sensor is also wired ORed before inputting.

- P33=1: Any of the drawers is open.

17. Rewriting flash memory

Below are the memory maps at the time of normal operation, shipping from the factory and IPL.

1. During normal operation (Fig. 17)
2. When leaving the factory (Fig. 18)

When a service PWB or AMRS PWB is inserted into an expansion I/O port, the PROM addresses on the service PWB are D00000H ~ DFFFFFh and 000000h ~ 007FFFFh (the map of D00000h ~ D07FFFh).

At this time, $\overline{\text{IPLON0}}$ signal input into the input port P10 of the CPU becomes "L" level.

Typical procedure for rewriting flash memory

If $\overline{\text{PLON0}}$ is found to be at "L" level by the program inside the 0page PROM, the contents in the PROM is written into the flash memory.

During normal operation

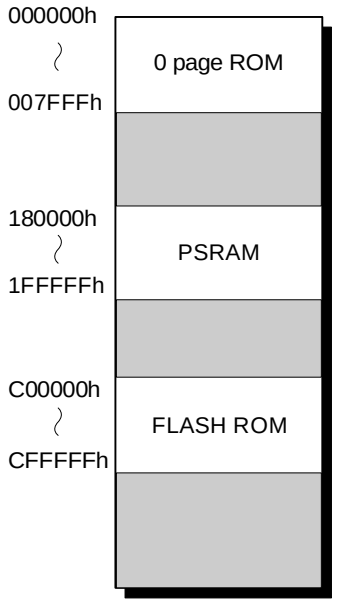


Fig. 17

When leaving the factory

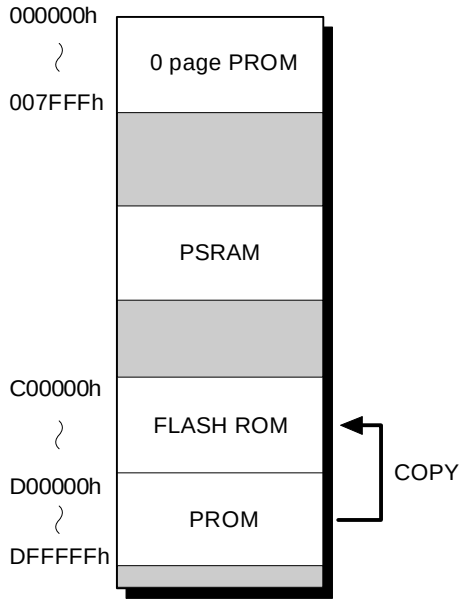
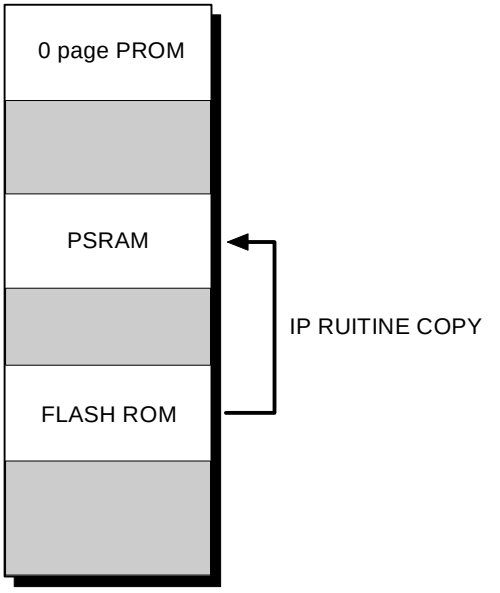


Fig. 18

3. During IPL

Typical procedure for rewriting flash memory

When $\overline{\text{IPLON1}}$ = "L" is detected at starting, the IPL routine is written into the PSRAM as shown in the figure below, and the IPL routine is used for rewriting the flash memory. (The $\overline{\text{IPLON1}}$ signal is controlled by the DIP switch and connected to the CPU P11.



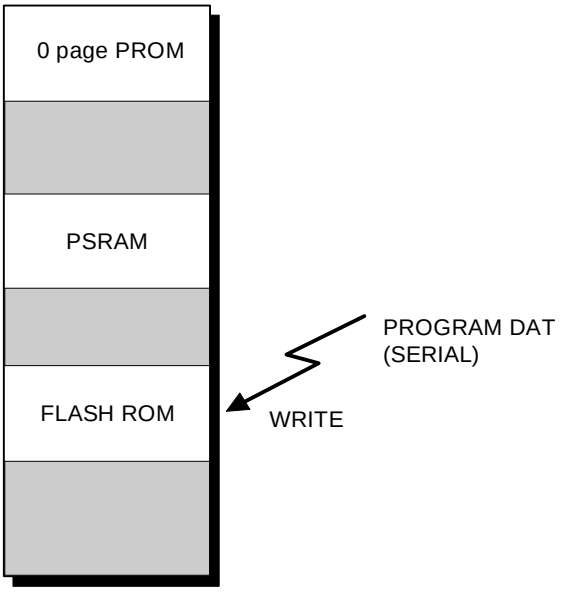


Fig. 19

18. IR communication

The ER-A750 has IR communication function which is softwarewisely compatible with the ER-A460. Data is exchanged with the MPCA7 using the channel 1 (SCI1) of the serial communication interface of the CPU.

18-1 CPU interface and modulator/demodulator

Here is its block diagram.

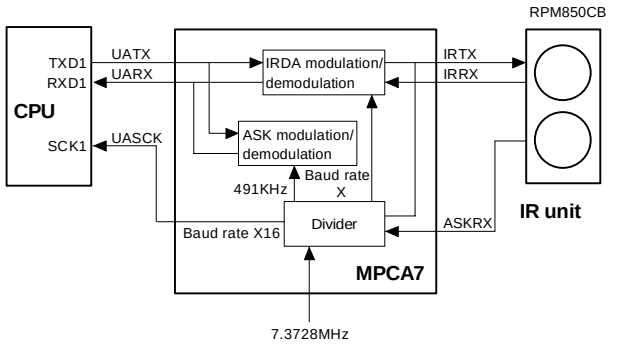


Fig. 20

19. SRN

The SRN of the ER-A750 is compatible with the ER-A6IN.

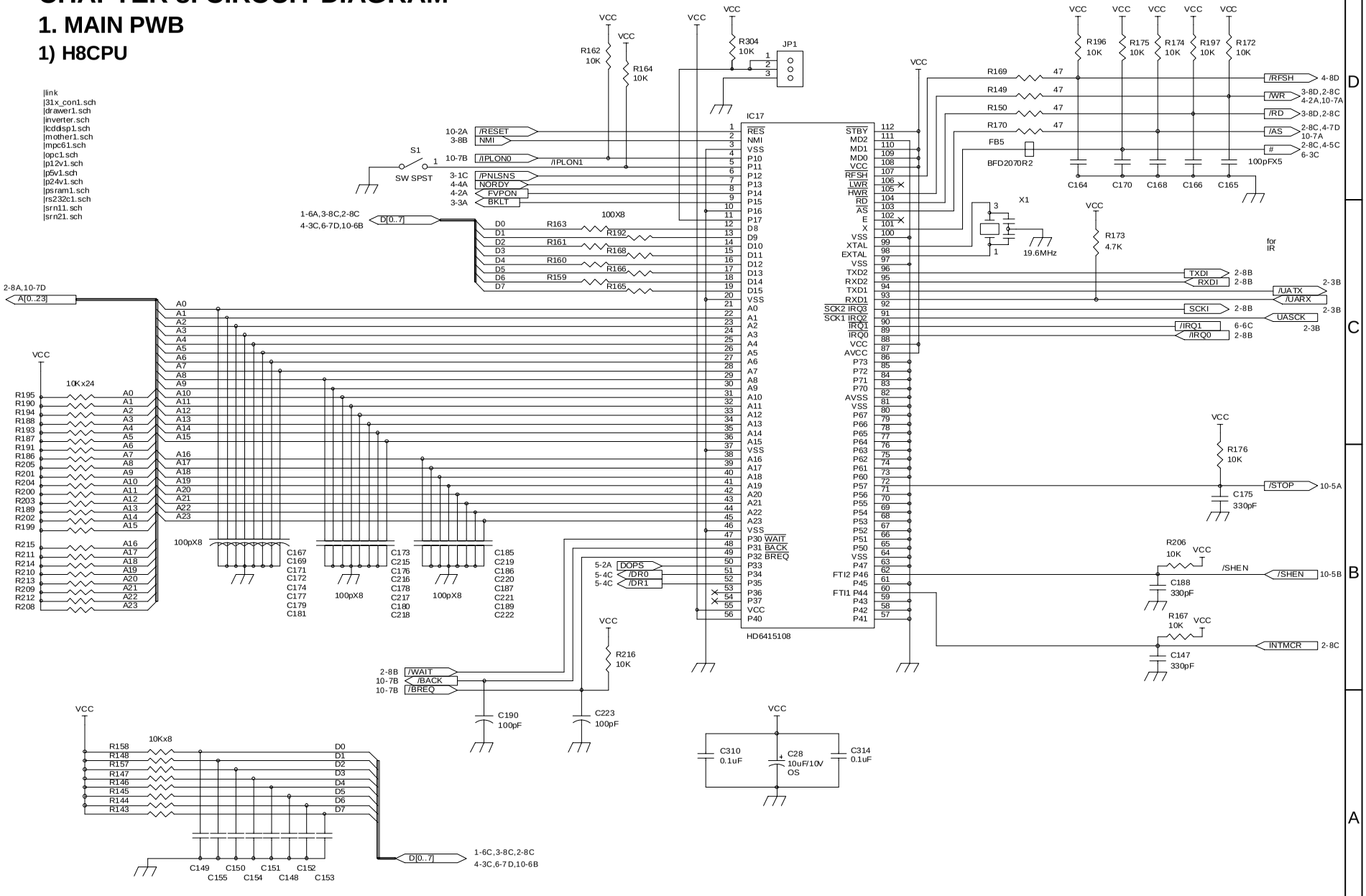
20. Standard RS232

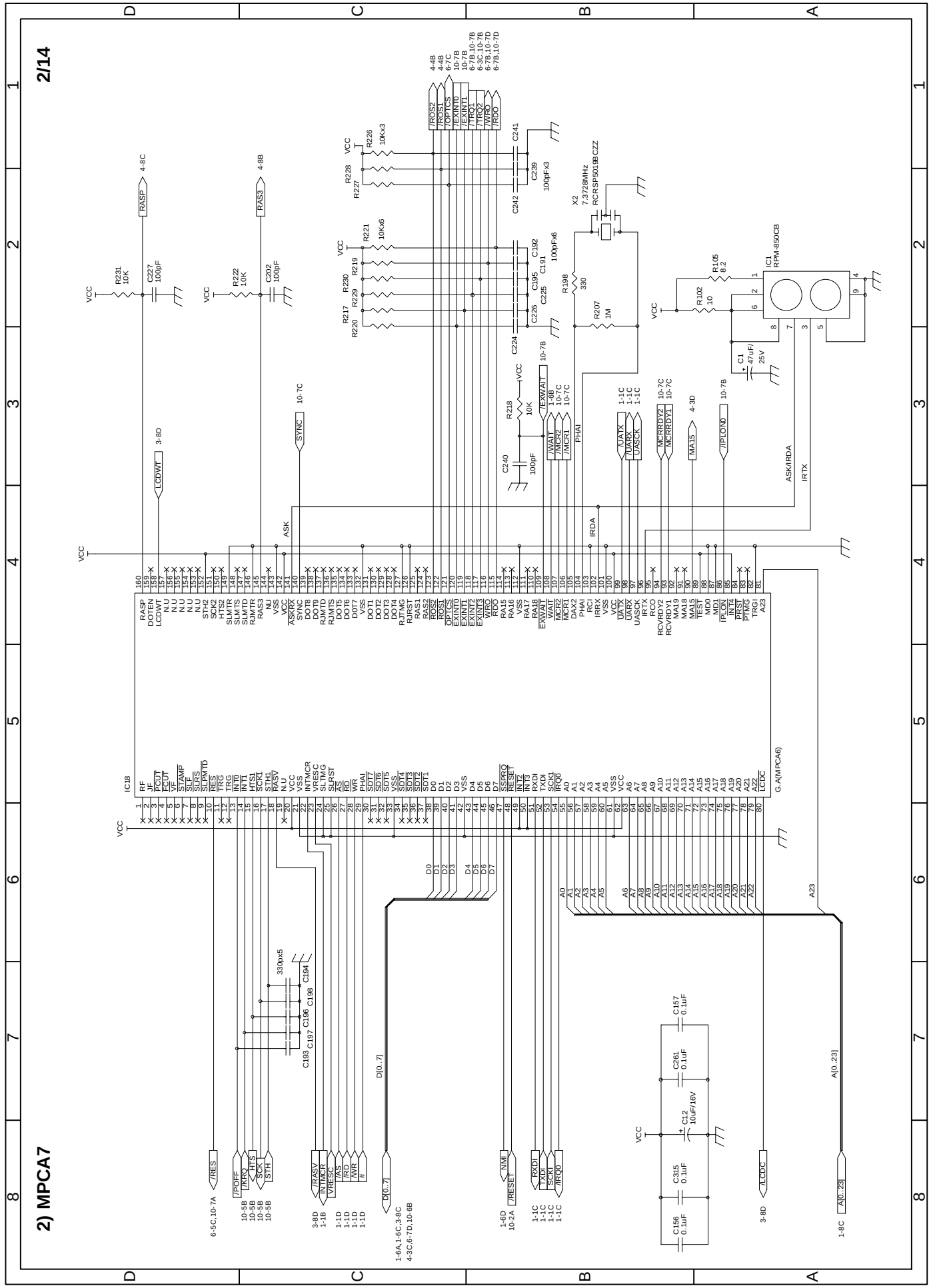
Two standard RS232 channels are compatible with the ER-A5RS. However, while the ER-A5RS uses the $\overline{IRQ2}$ terminal of the CPU for interruption of the RS232, the ER-A750 cannot use the $\overline{IRQ1}$ terminal instead of it. (The $\overline{IRQ2}$ terminal is used for IR as the SCK1 terminal.)

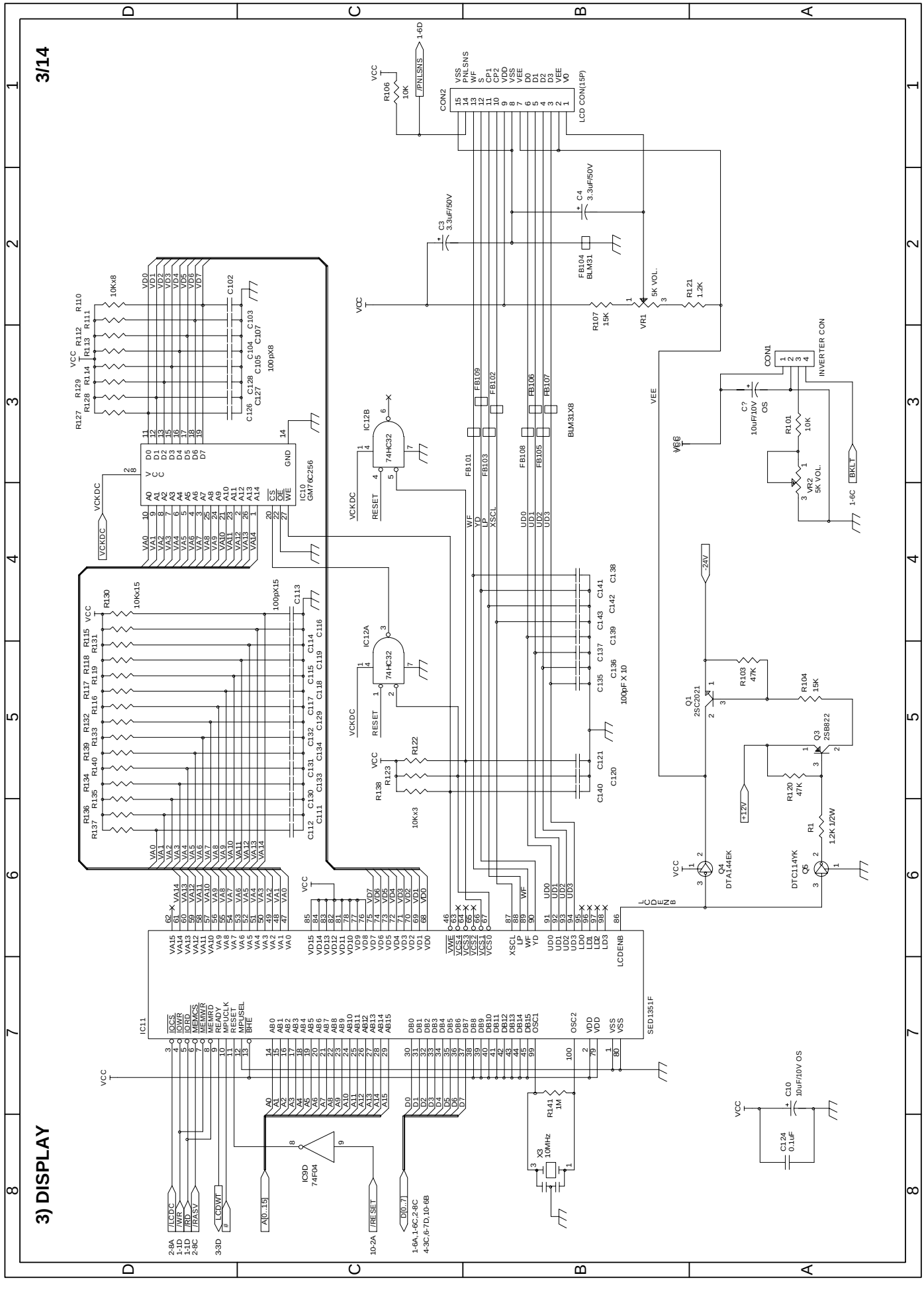
CHAPTER 8. CIRCUIT DIAGRAM

1. MAIN PWB

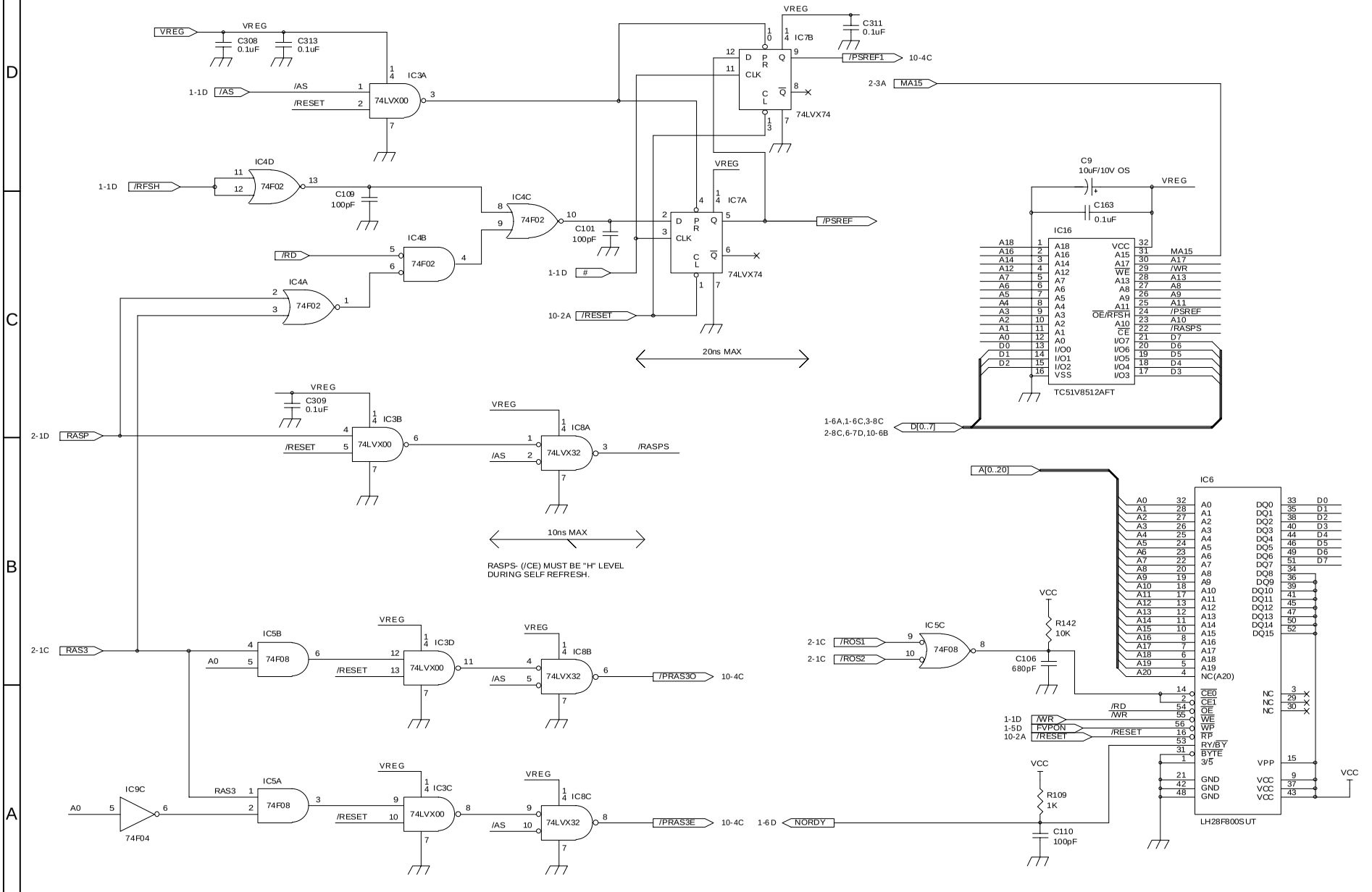
1) H8CPU



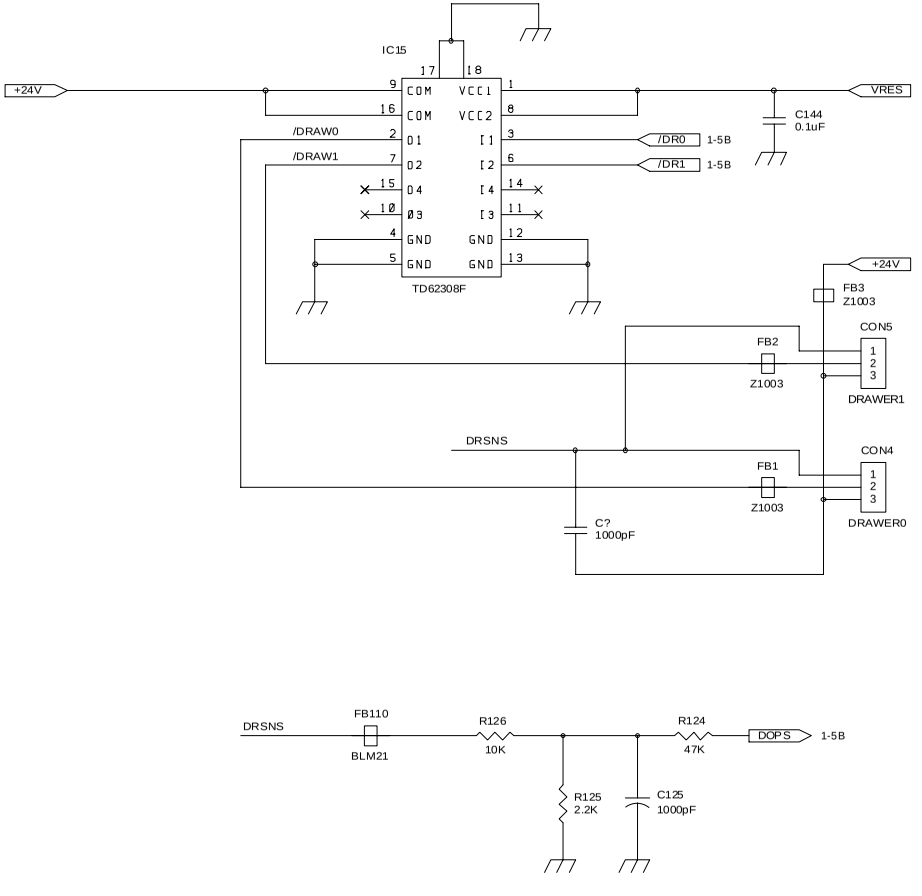

2/14
2) MPCA7
IC1B
G.A(MPCA6)
IC1
RPM-850CB
X2
7.3728MHz
RCRSP501BCZZ
VCC
SYNC
ASK
IRDA
ASK/IRDA
IRTX
PHAI
LCDWT
RASP
RAS3
/RESET
NMI
/TRESET
/RXDI
/TXDI
/SCKI
/IRQ0
/TRXD
/TRRQ
/HTS
/SCK
/STH
/TPOFF
/TRASV
/INTMCR
/VRESC
/TAS
/TRD
/WR
/#
/TEXWAIT
/WAIT
/MCR2
/MCR1
/UATX
/UARX
UASCK
MCRRDY2
MCRRDY1
/IPLON0
MA15
/TROS2
/TROS1
/TOPTCS
/TEXINT0
/TEXINT1
/TRRQ1
/TRRQ2
/TWRO
/TRDO
LCDC
A[0..23]
D[0..7]
RES
1-8C
3-8D
6-5C,10-7A
1-6D
10-2A
1-16A,16C,3-8C
4-3C,6-7D,10-6B
10-5B
1-1D
1-1C
10-7C
10-7B
4-8C
4-8B
4-8A
4-8B
4-3D
6-7C
6-3C,10-7B
6-7B,10-7D
1-6B
1-1C
R231 10K
R222 10K
R221 10Kx6
R226 10Kx3
R218 10K
R198 330
R207 1M
R102 10
R105 8.2
C227 100pF
C202 100pF
C192 100pFx6
C191 100pF
C195
C225
C226
C224
C240 100pF
C241
C239 100pFx3
C242
C1 47uF/25V
C156 0.1uF
C315 0.1uF
C12 10uF/16V
C261 0.1uF
C157 0.1uF
330pFx5
C193
C197
C196
C198
C194
R217
R220
R230
R229
R219
R227
R228


3/14
3) DISPLAY
IC11
SED1351F
IC10
GM76C256
CON2
LCD CON(15P)
CON1
INVERTER CON
IC12A
IC12B
74HC32
IC9D
74F04
Q1
2SC2021
Q3
2SB822
Q4
DTA144EK
Q5
DTC114YK
X3
10MHz
VR1
5K VOL.
VR2
5K VOL.
BLM31X8
/LCDC
/WR
/RD
/RASV
LCDWT
/RESET
A[0..15]
D[0..7]
VCC
VCKDC
-24V
+12V
VEE
LCDENB
/PNLSNS
BKLT

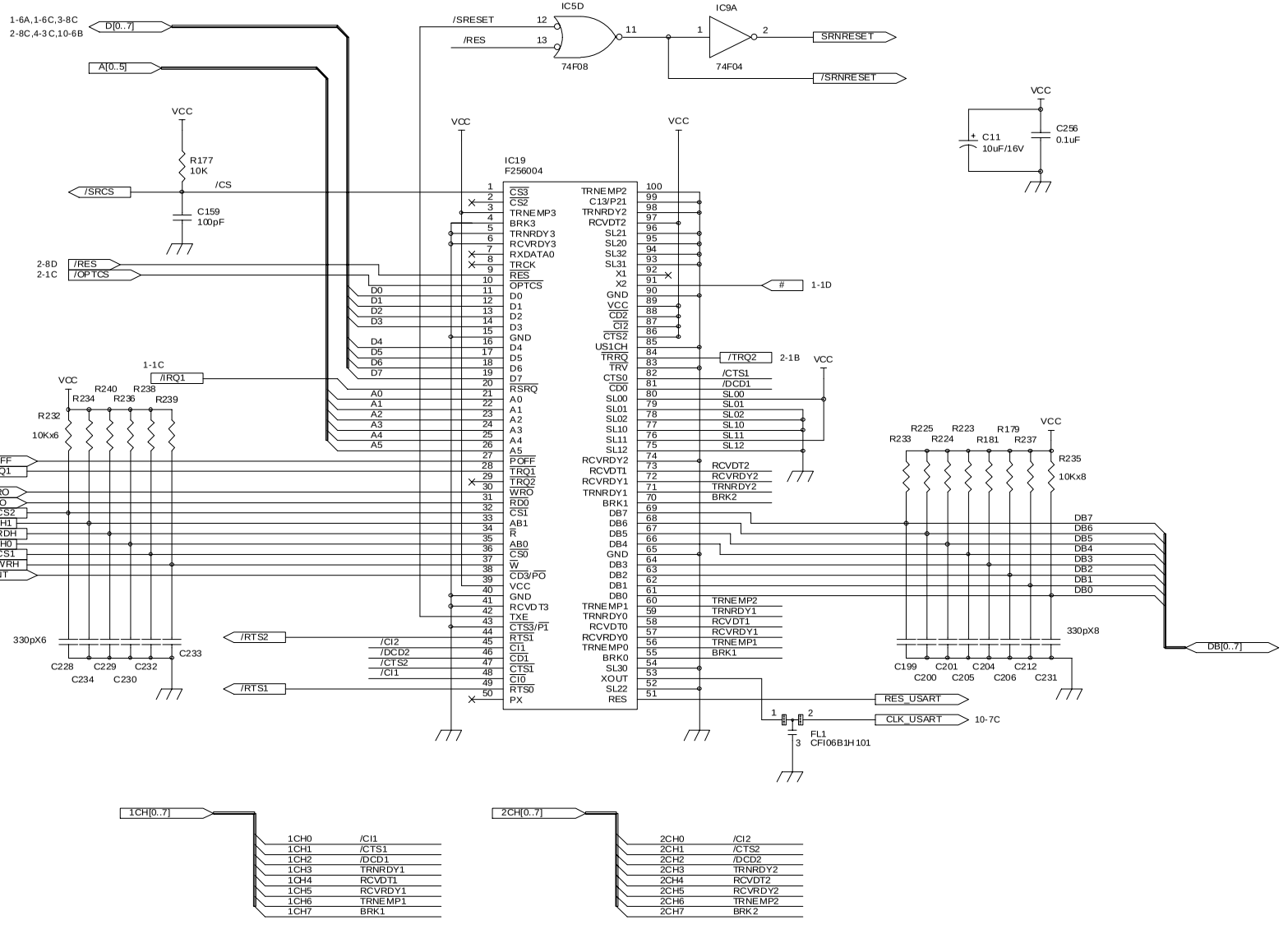
4) ROM/RAM


VREG
C308 0.1uF
C313 0.1uF
IC3A
74LVX00
1-1D /AS
/AS
/RESET
IC7B
74LVX74
C311 0.1uF
/PSREF1 10-4C
2-3A MA15
IC4D
74F02
1-1D /RFSH
C109 100pF
IC4C
C101 100pF
IC4B
/RD
IC4A
1-1D #
10-2A /RESET
IC7A
/PSREF
20ns MAX
C9 10uF/10V OS
C163 0.1uF
IC16
TC51V8512AFT
1-6A,1-6C,3-8C
2-8C,6-7D,10-6B
D[0..7]
C309 0.1uF
IC3B
2-1D RASP
IC8A
/RASPS
10ns MAX
RASPS- (/CE) MUST BE "H" LEVEL
DURING SELF REFRESH.
A[0..20]
IC6
LH28F800SUT
IC5B
74F08
2-1C RAS3
A0
IC3D
IC8B
/PRAS3O 10-4C
IC5C
2-1C /ROS1
2-1C /ROS2
R142 10K
C106 680pF
/RD
/WR
1-1D /WR
1-5D FVPON
10-2A /RESET
IC9C
74F04
IC5A
IC3C
IC8C
/PRAS3E 10-4C
1-6D NORDY
R109 1K
C110 100pF
VCC
GND

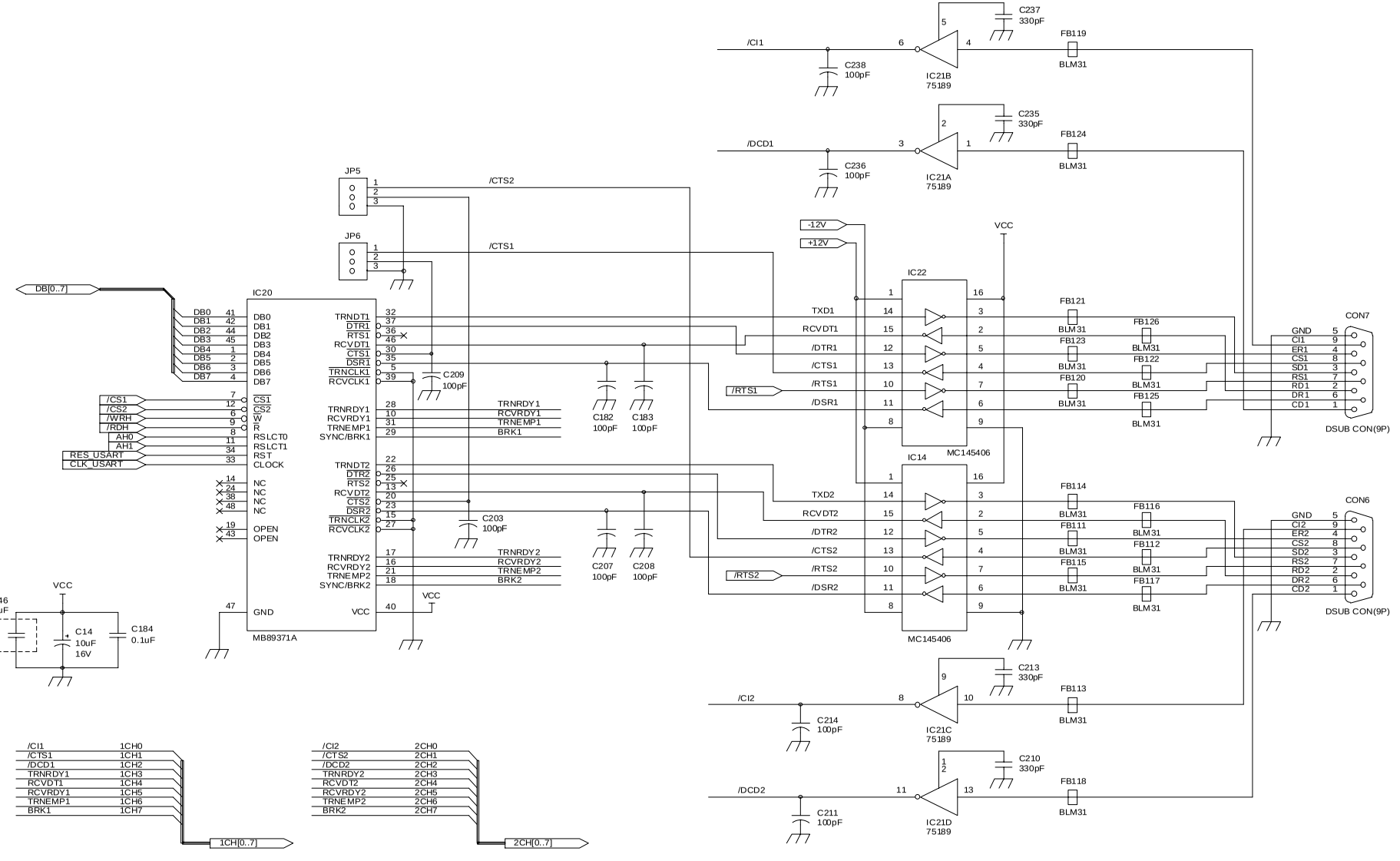
5) DRAWER

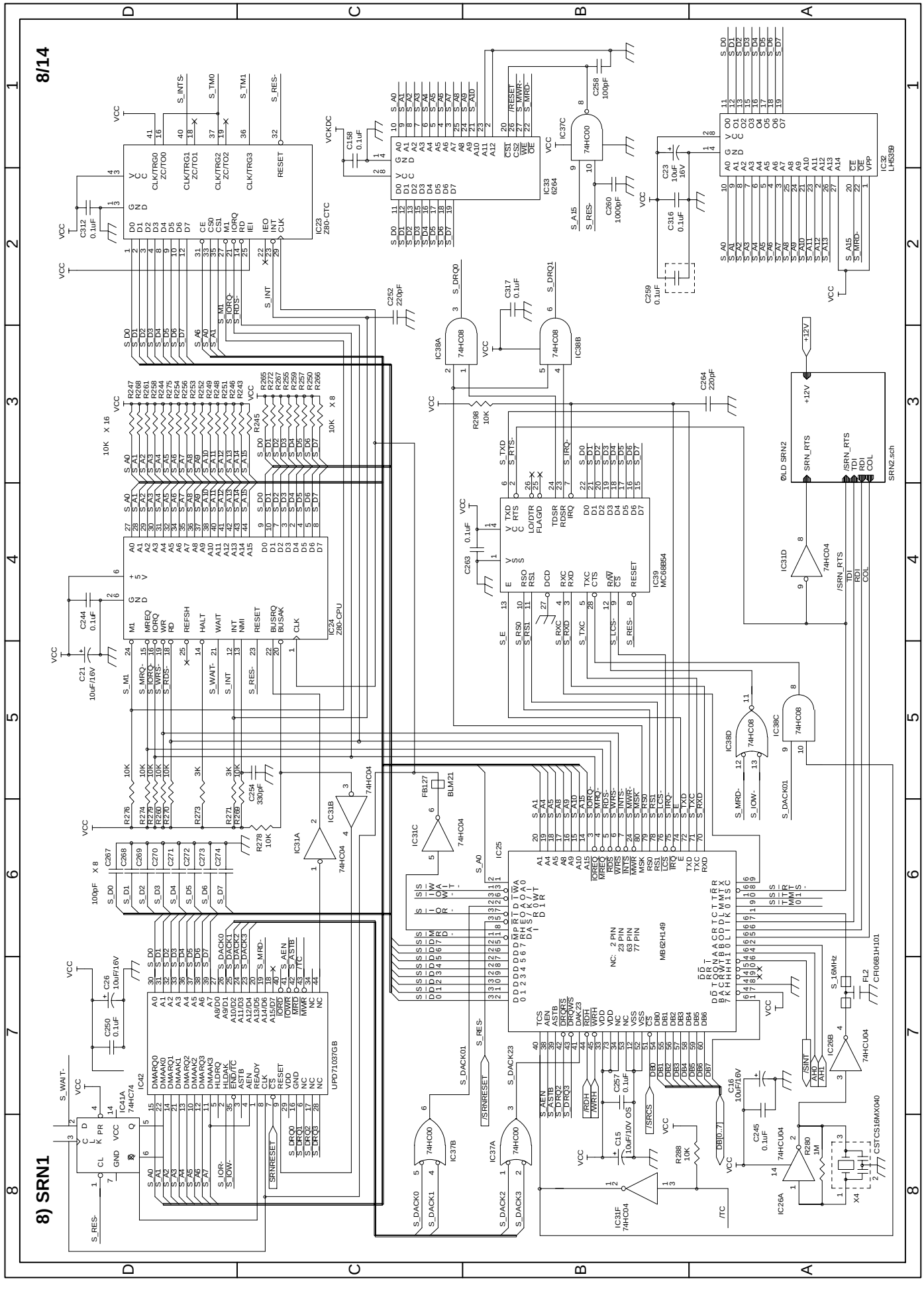

IC15
+24V
VRES
C144
0.1uF
/DRAW0
/DRAW1
/DR0
1-5B
/DR1
1-5B
TD62308F
+24V
FB3
Z1003
CON5
FB2
Z1003
DRAWER1
DRSNS
CON4
FB1
Z1003
DRAWER0
C?
1000pF
DRSNS
FB110
BLM21
R126
10K
R124
47K
DOPS
1-5B
R125
2.2K
C125
1000pF

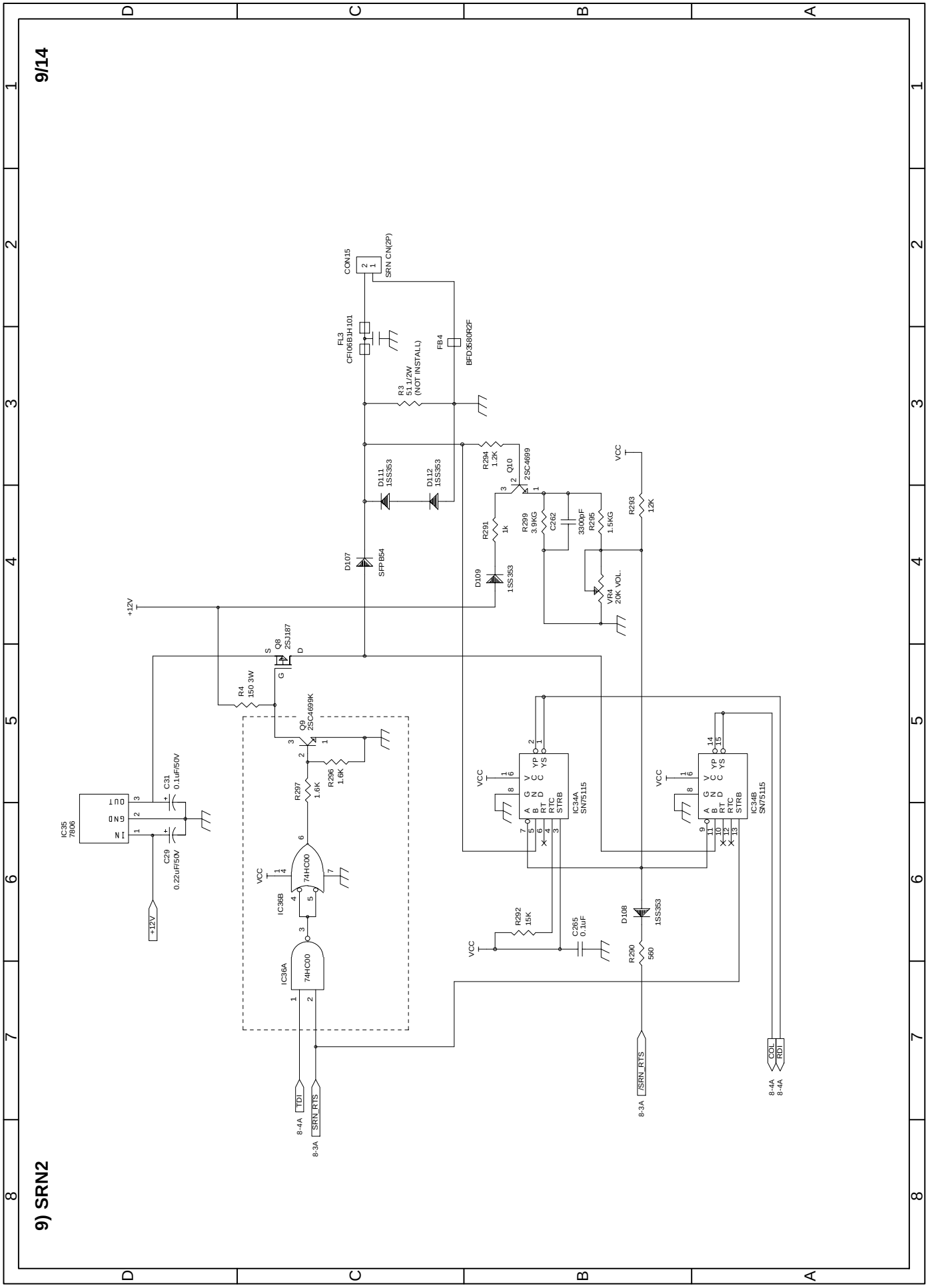
6) OPC1


1-6A,1-6C,3-8C
2-8C,4-3C,10-6B
D[0..7]
A[0..5]
/SRESET
/RES
IC5D
74F08
IC9A
74F04
SRNRESET
/SRNRESET
VCC
R177
10K
/CS
/SRCS
C159
100pF
2-8D
2-1C
/RES
/OPTCS
C11
10uF/16V
C256
0.1uF
IC19
F256004
1-1C
/IRQ1
R234
R240
R238
R236
R239
R232
10Kx6
/POFF
/TRQ1
/WRO
/RDO
/CS2
AH1
/RDH
AH0
/CS1
/WRH
/SINT
330pX6
C228
C229
C232
C233
C234
C230
/RTS2
/RTS1
/CI2
/DCD2
/CTS2
/CI1
/TRQ2
2-1B
/CTS1
/DCD1
SL00
SL01
SL02
SL10
SL11
SL12
RCVDT2
RCVRDY2
TRNRDY2
BRK2
#
1-1D
R225
R223
R179
R233
R224
R181
R237
R235
10Kx8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
330pX8
C199
C201
C204
C212
C200
C205
C206
C231
DB[0..7]
RES_USART
CLK_USART
10-7C
FL1
CFI06B1H101
1CH[0..7]
1CH0 /CI1
1CH1 /CTS1
1CH2 /DCD1
1CH3 TRNRDY1
1CH4 RCVDT1
1CH5 RCVRDY1
1CH6 TRNEMP1
1CH7 BRK1
2CH[0..7]
2CH0 /CI2
2CH1 /CTS2
2CH2 /DCD2
2CH3 TRNRDY2
2CH4 RCVDT2
2CH5 RCVRDY2
2CH6 TRNEMP2
2CH7 BRK2

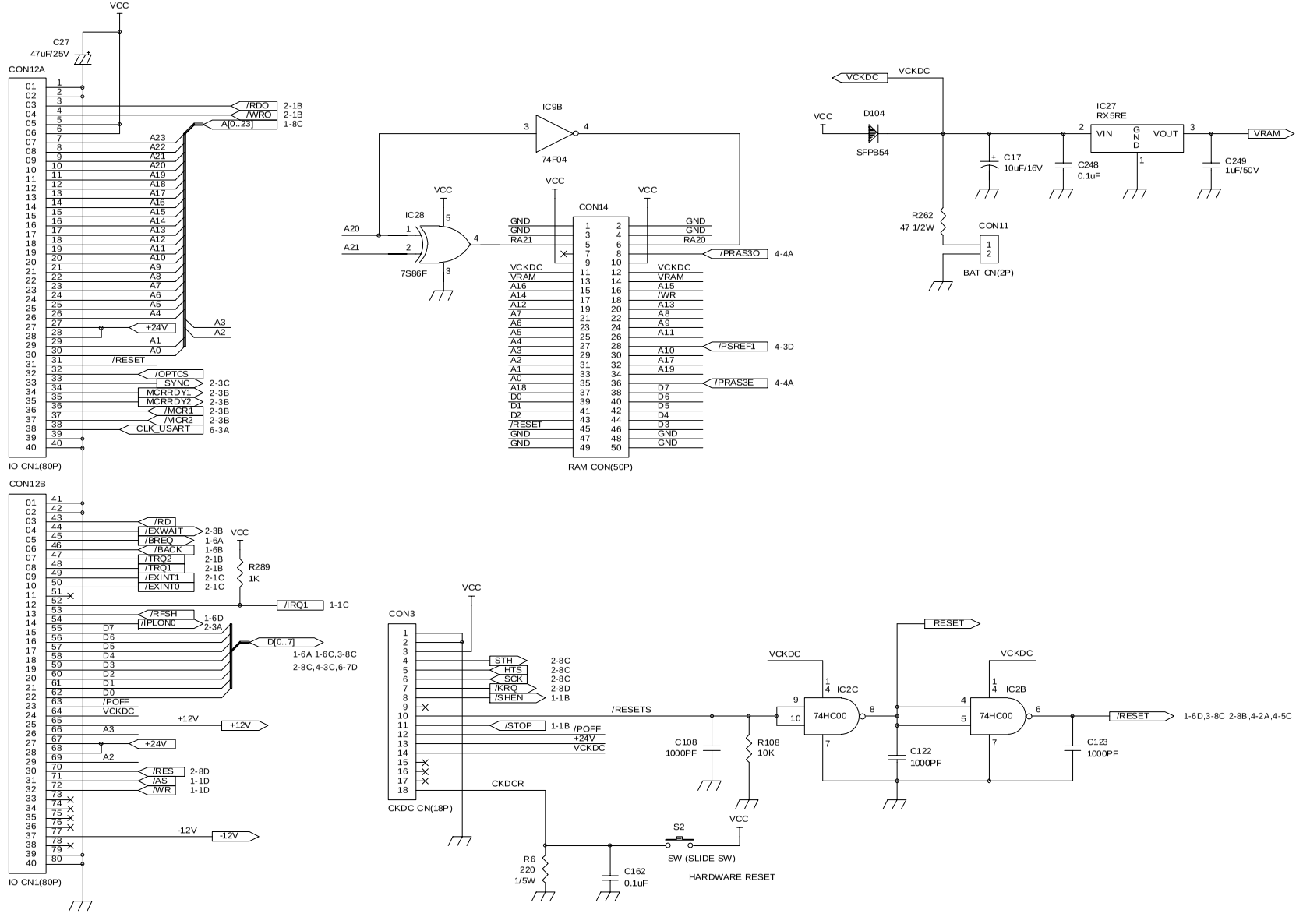
7) RS232


JP5
JP6
/CTS2
/CTS1
DB[0..7]
IC20
MB89371A
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
/CS1 /CS2 /WRH /RDH AH0 AH1 RES_USART CLK_USART
CS1 CS2 W R RSLCT0 RSLCT1 RST CLOCK
NC NC NC NC OPEN OPEN
GND VCC
TRNDT1 DTR1 RTS1 RCVDT1 CTS1 DSR1 TRNCLK1 RCVCLK1
TRNRDY1 RCVRDY1 TRNEMP1 SYNC/BRK1
TRNDT2 DTR2 RTS2 RCVDT2 CTS2 DSR2 TRNCLK2 RCVCLK2
TRNRDY2 RCVRDY2 TRNEMP2 SYNC/BRK2
C209 100pF
C203 100pF
C182 100pF
C183 100pF
C207 100pF
C208 100pF
C246 0.1uF
C14 10uF 16V
C184 0.1uF
VCC
/CI1 /CTS1 /DCD1 TRNRDY1 RCVDT1 RCVRDY1 TRNEMP1 BRK1
1CH0 1CH1 1CH2 1CH3 1CH4 1CH5 1CH6 1CH7
1CH[0..7]
/CI2 /CTS2 /DCD2 TRNRDY2 RCVDT2 RCVRDY2 TRNEMP2 BRK2
2CH0 2CH1 2CH2 2CH3 2CH4 2CH5 2CH6 2CH7
2CH[0..7]
-12V
+12V
IC22
MC145406
TXD1 RCVDT1 /DTR1 /CTS1 /RTS1 /DSR1
/RTS1
IC14
MC145406
TXD2 RCVDT2 /DTR2 /CTS2 /RTS2 /DSR2
/RTS2
/CI1
/DCD1
/CI2
/DCD2
C238 100pF
C236 100pF
C214 100pF
C211 100pF
IC21B 75189
IC21A 75189
IC21C 75189
IC21D 75189
C237 330pF
C235 330pF
C213 330pF
C210 330pF
FB119 BLM31
FB124 BLM31
FB121 BLM31
FB126 BLM31
FB123 BLM31
FB122 BLM31
FB120 BLM31
FB125 BLM31
FB114 BLM31
FB116 BLM31
FB111 BLM31
FB112 BLM31
FB115 BLM31
FB117 BLM31
FB113 BLM31
FB118 BLM31
CON7
GND CI1 ER1 CS1 SD1 RS1 RD1 DR1 CD1
DSUB CON(9P)
CON6
GND CI2 ER2 CS2 SD2 RS2 RD2 DR2 CD2
DSUB CON(9P)

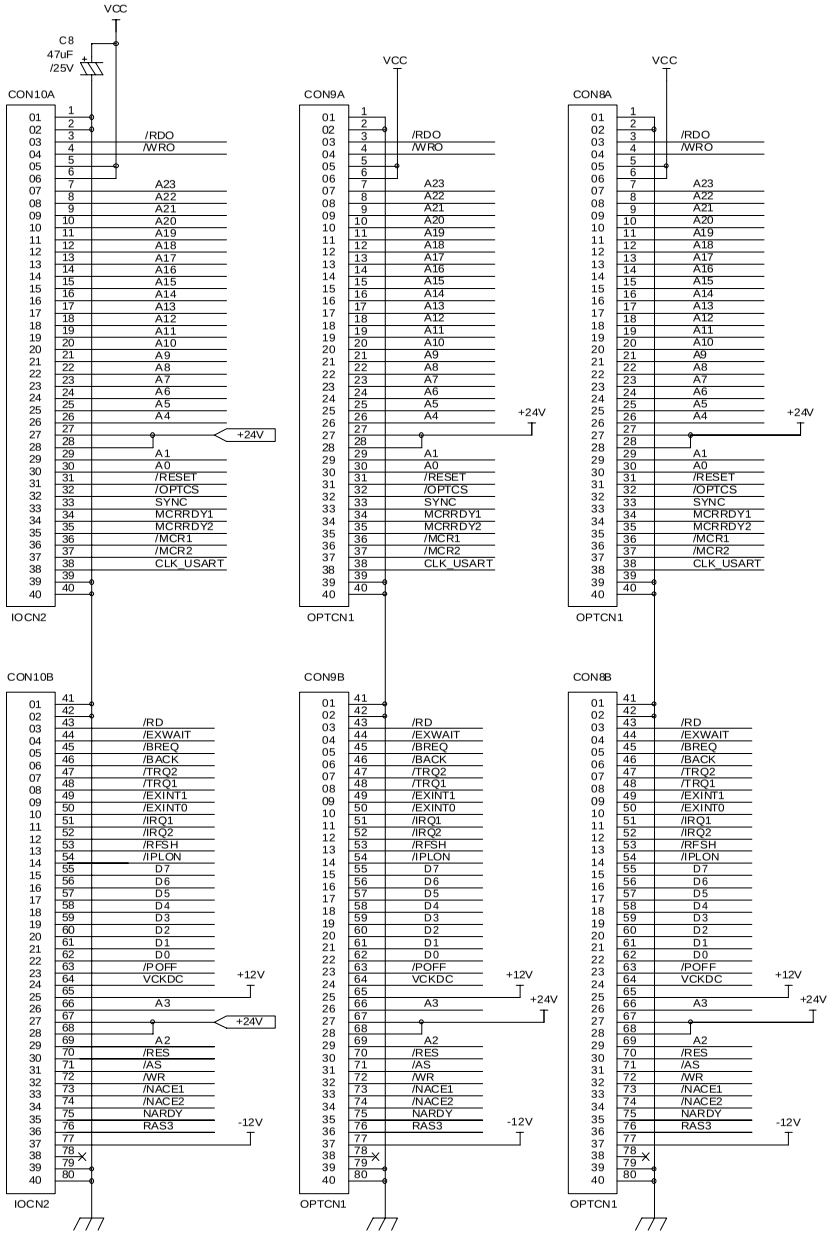

8/14
8) SRN1
SRN2.sch


9/14
9) SRN2
CON15
SRN CN(2P)
FL3
CFI0603H101
FB4
BFD3580R2F
R3
51 1/2W
(NOT INSTALL)
D111
1SS353
D112
1SS353
R294
1.2K
Q10
2SC4699
D107
SFPB54
R291
1k
D109
1SS353
R299
3.9KG
C262
3300pF
R295
1.5KG
VR4
20K VOL.
R293
12K
VCC
+12V
Q8
2SJ187
R4
150 3W
Q9
2SC4699K
R297
1.6K
R296
1.6K
IC35
7806
IN
GND
OUT
C31
0.1uF/50V
C29
0.22uF/50V
+12V
IC36B
74HC00
IC36A
74HC00
IC34A
SN75115
IC34B
SN75115
A
B
GND
RT
RTC
STRB
VCC
R292
15K
C265
0.1uF
D108
1SS353
R290
560
TDI
SRN RTS
/SRN RTS
COL
RDI
8-4A
8-3A
8 – 9

10) MAIN CONNECTOR

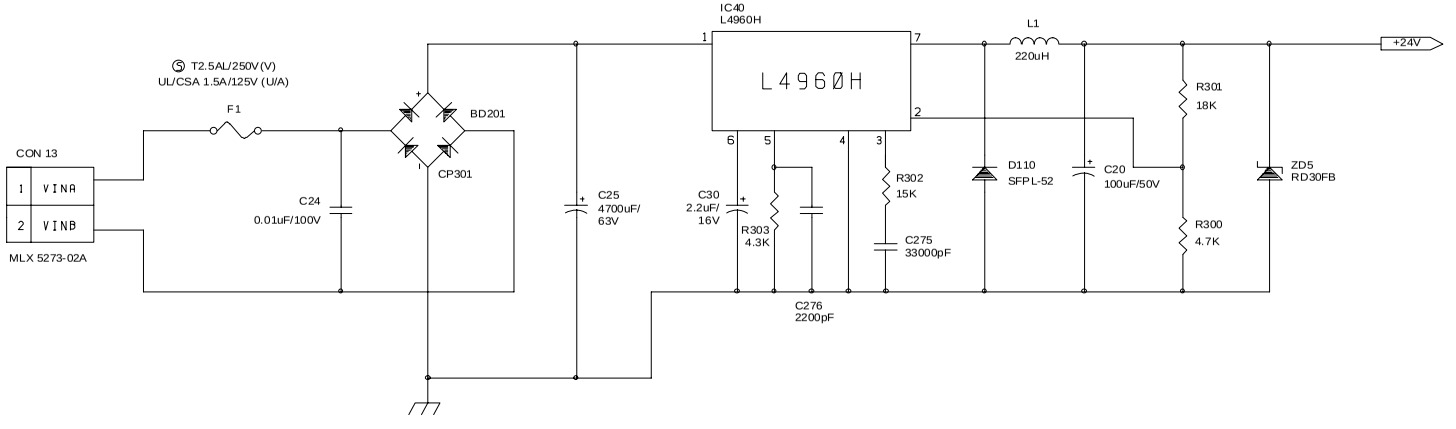


CAUTION !! IF YOU WILL DEBUG THE NEW CKDC-PWB THEN JP 1PIN AND 2PIN MUST SHORT.


VCC
C8
47uF
/25V
CON10A
IOCN2
CON9A
OPTCN1
CON8A
OPTCN1
CON10B
IOCN2
CON9B
OPTCN1
CON8B
OPTCN1
/RDO
/WRO
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
+24V
A1
A0
/RESET
/OPTCS
SYNC
MCRRDY1
MCRRDY2
/MCR1
/MCR2
CLK_USART
/RD
/EXWAIT
/BREQ
/BACK
/TRQ2
/TRQ1
/EXINT1
/EXINT0
/IRQ1
/IRQ2
/RFSH
/IPLON
D7
D6
D5
D4
D3
D2
D1
D0
/POFF
VCKDC
+12V
A3
+24V
A2
/RES
/AS
/WR
/NACE1
/NACE2
NARDY
RAS3
-12V

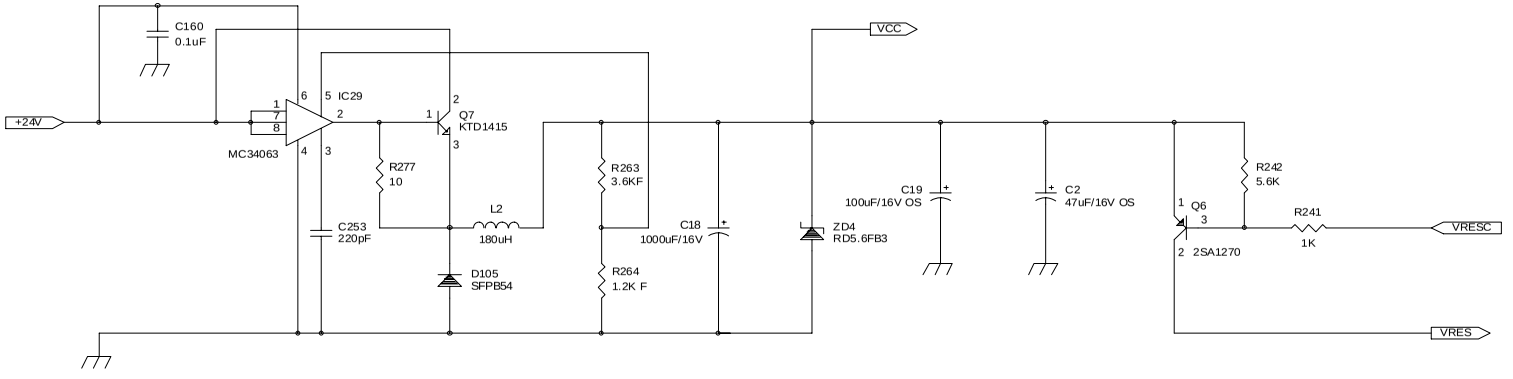
12) +24V POWER CIRCUIT

12/14

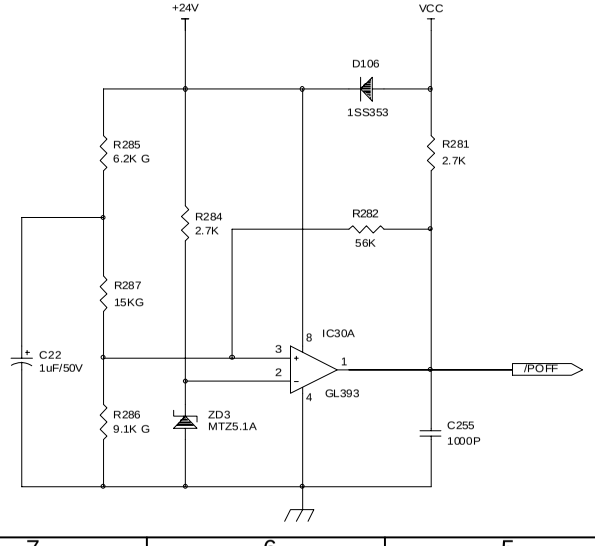


13) +5V, /POFF CIRCUIT

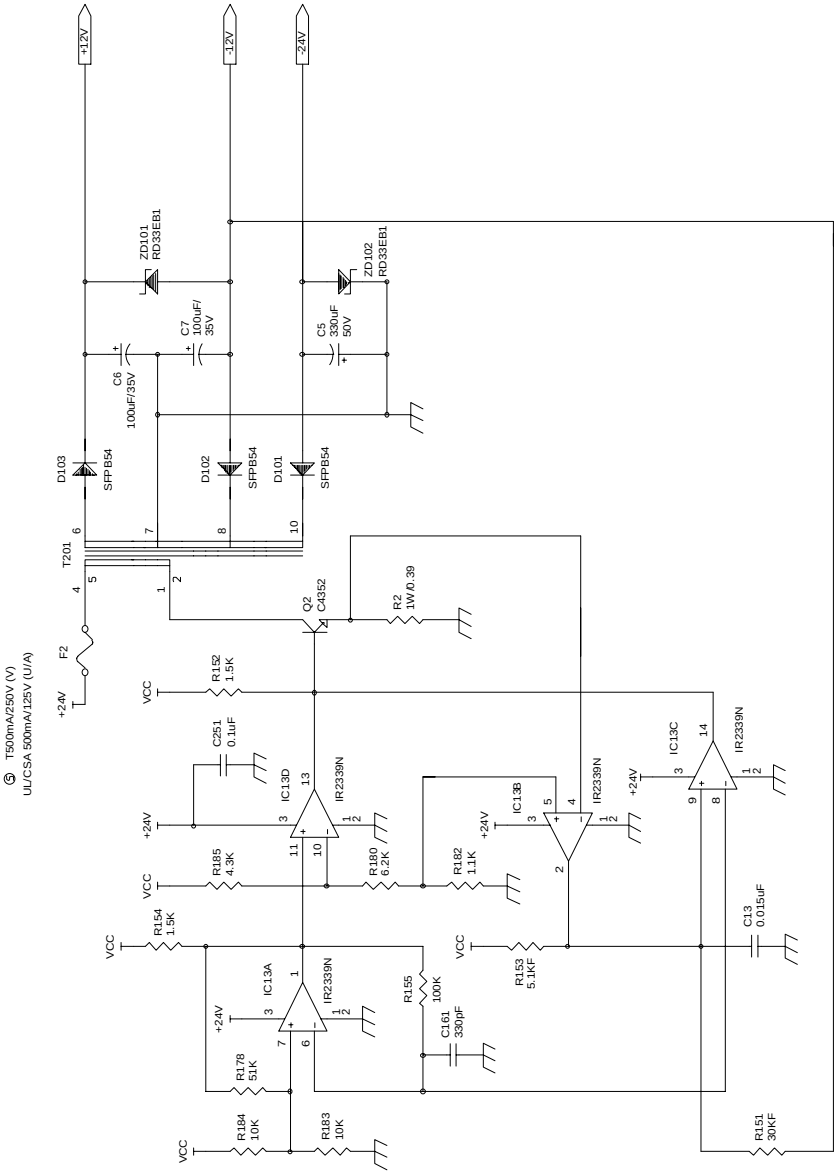
[+5V POWER CIRCUIT]



[POFF CIRCUIT]

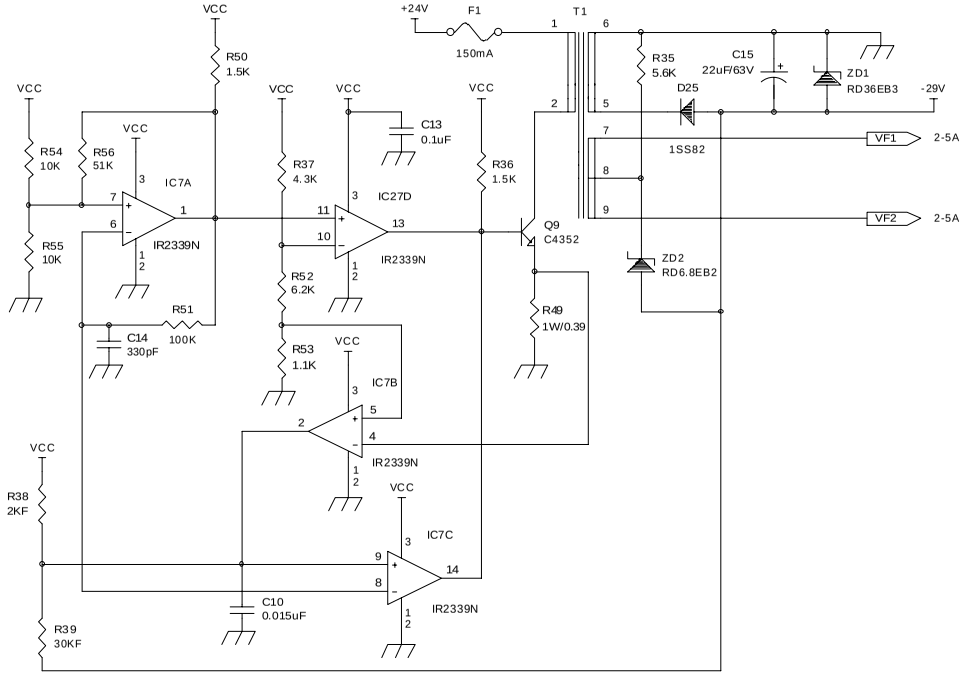


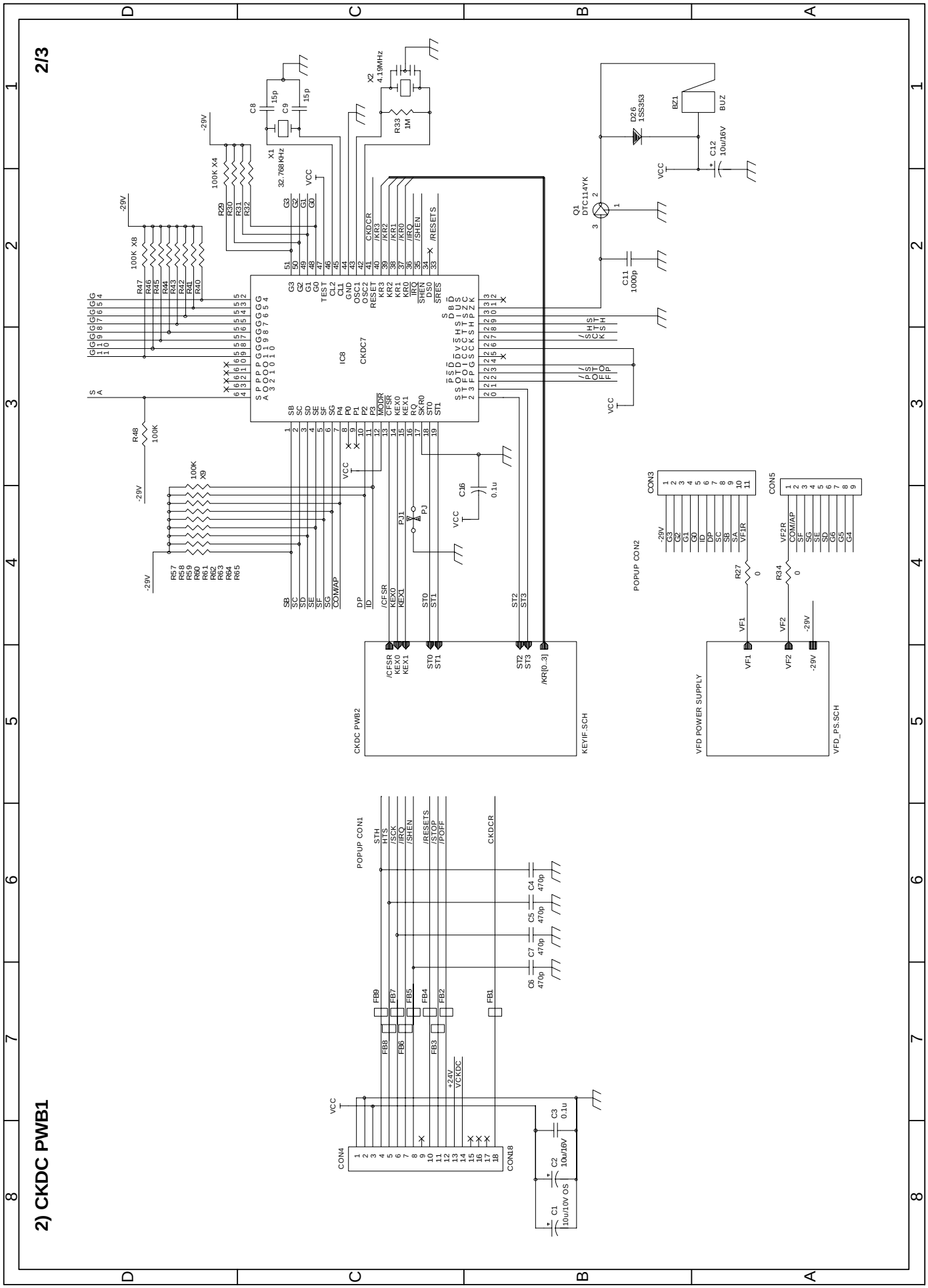
14) DC-DC CNV CIRCUIT

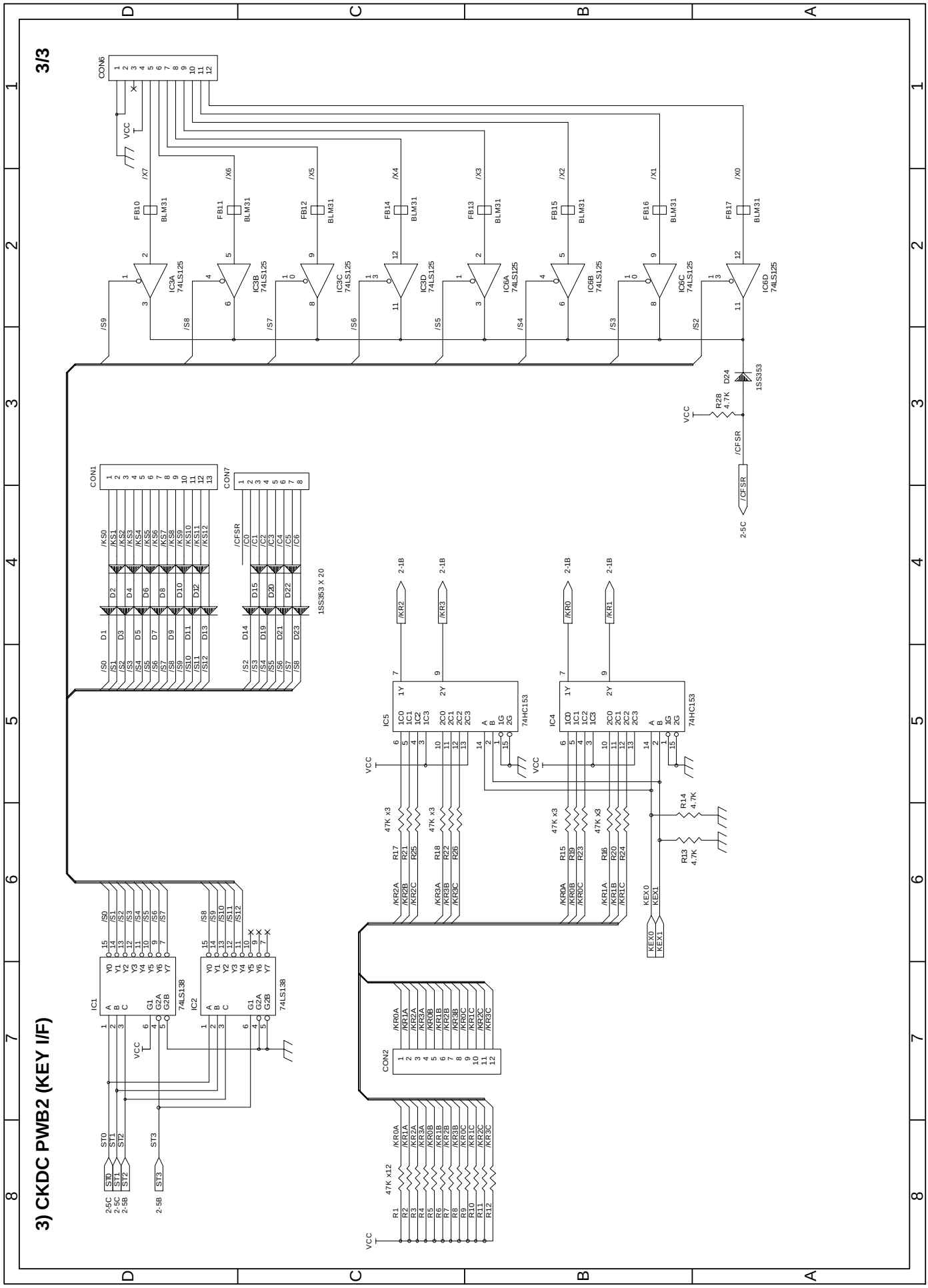


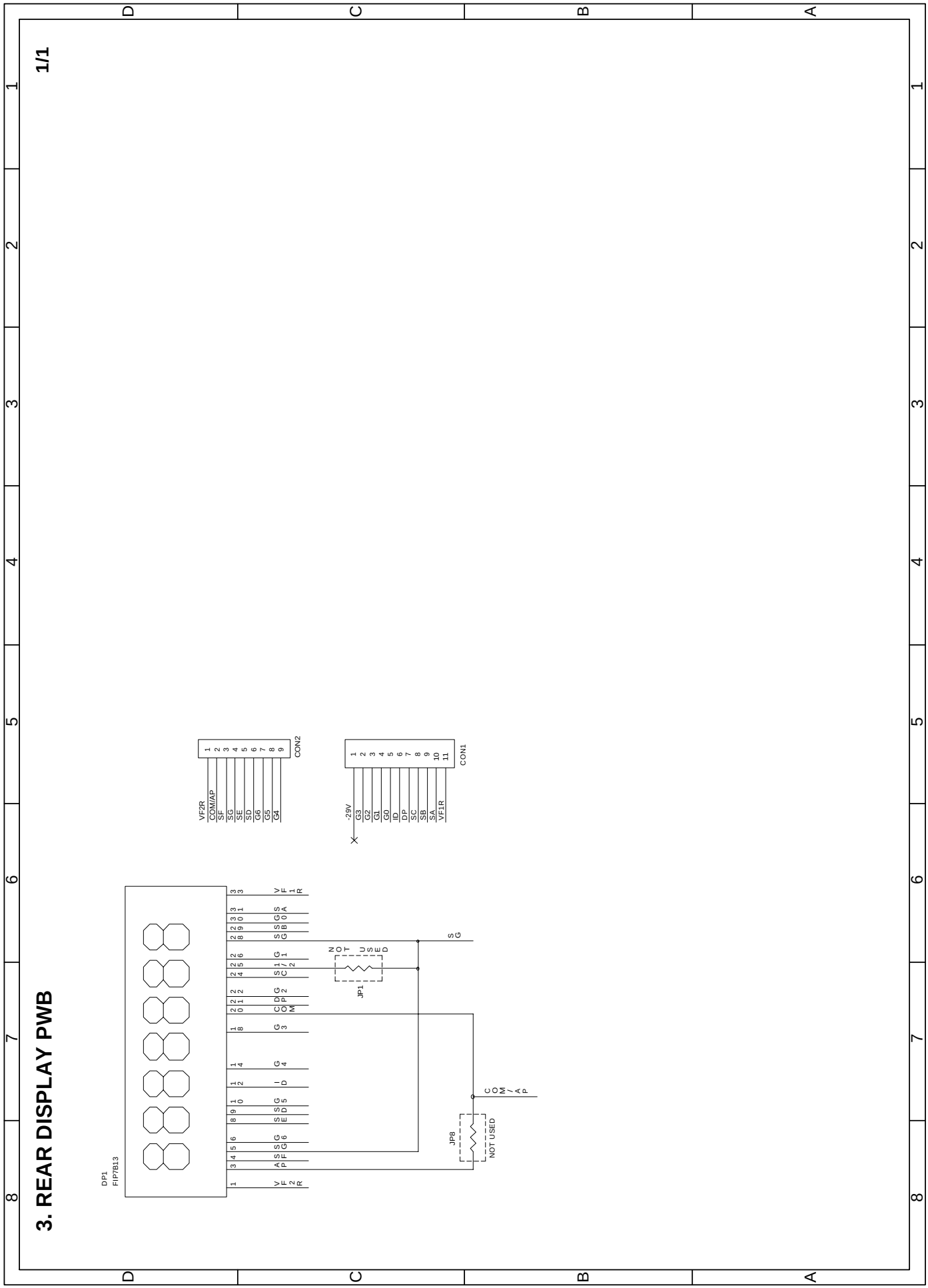
2. CKDC PWB

1) VFD POWER SUPPLY



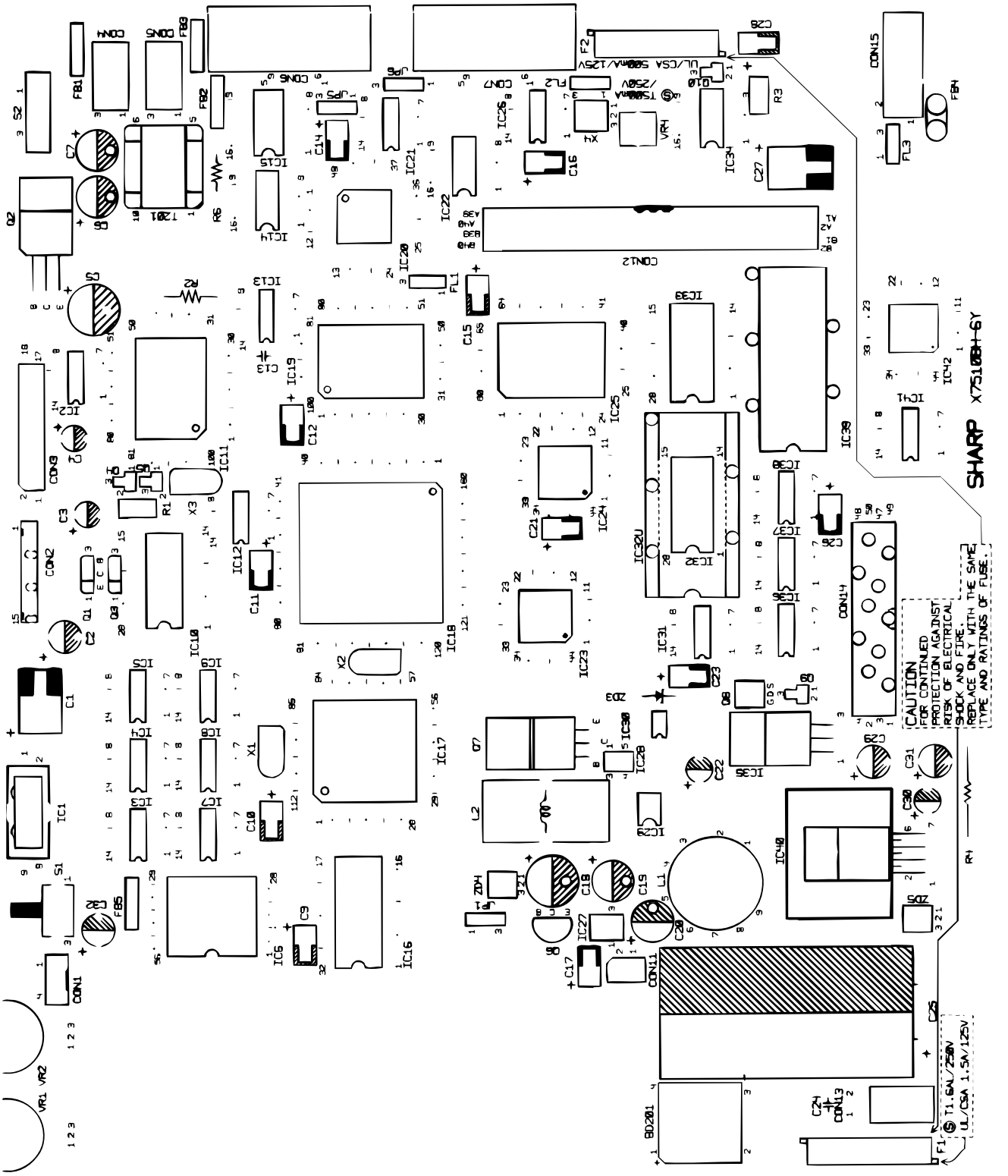

2/3
2) CKDC PWB1
IC8
CKDC7
X1
32.768KHz
X2
4.19MHz
C8
15p
C9
15p
R33
1M
R29
R30
R31
R32
100K X4
-29V
VCC
R47
R46
R45
R44
R43
R42
R41
R40
100K X8
R48
100K
100K
X9
R57
R58
R59
R60
R61
R62
R63
R64
R65
C16
0.1u
PJ31
PJ
Q1
DTC114YK
C11
1000p
D26
1SS353
BZ1
BUZ
C12
10u/16V
CKDCR
/KR3
/KR2
/KR1
/KR0
/IRQ
/SHEN
/RESETS
/SHCK
/SHTH
/PSTOFF
CKDC PWB2
KEY/F.SCH
/CFSR
KEX0
KEX1
ST0
ST1
ST2
ST3
/KR[0..3]
POPUP CON2
CON3
CON5
R27
R34
VF1R
VF2R
COM/AP
VFD POWER SUPPLY
VFD_PS.SCH
POPUP CON1
STH
/SCK
/IRQ
/SHEN
/RESETS
/STOP
/POFF
C4
C5
C7
C6
470p
FB1
FB2
FB3
FB4
FB5
FB6
FB7
FB8
FB9
+24V
VCKDC
CON4
CON18
C3
0.1u
C2
10u/16V
C1
10u/10V OS


3/3
3) CKDC PWB2 (KEY I/F)
CON6
VCC
/X7
/X6
/X5
/X4
/X3
/X2
/X1
/X0
FB10
FB11
FB12
FB14
FB13
FB15
FB16
FB17
BLM31
IC3A 74LS125
IC3B 74LS125
IC3C 74LS125
IC3D 74LS125
IC6A 74LS125
IC6B 74LS125
IC6C 74LS125
IC6D 74LS125
/S9
/S8
/S7
/S6
/S5
/S4
/S3
/S2
D24
1SS353
R28 4.7K
/CFSR
2-5C
CON1
CON7
/KS0
/KS1
/KS2
/KS3
/KS4
/KS5
/KS6
/KS7
/KS8
/KS9
/KS10
/KS11
/KS12
/CFSR
/C0
/C1
/C2
/C3
/C4
/C5
/C6
1SS353 X 20
/JKR2
/JKR3
/JKR0
/JKR1
2-1B
IC5
IC4
74HC153
47K x3
R17
R21
R25
R18
R22
R26
R15
R19
R23
R16
R20
R24
/JKR2A
/JKR2B
/JKR2C
/JKR3A
/JKR3B
/JKR3C
/JKR0A
/JKR0B
/JKR0C
/JKR1A
/JKR1B
/JKR1C
R14 4.7K
R13 4.7K
KEX0
KEX1
IC1
IC2
74LS138
/S0
/S1
/S2
/S3
/S4
/S5
/S6
/S7
/S8
/S9
/S10
/S11
/S12
ST0
ST1
ST2
ST3
2-5C
2-5B
CON2
47K x12
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12

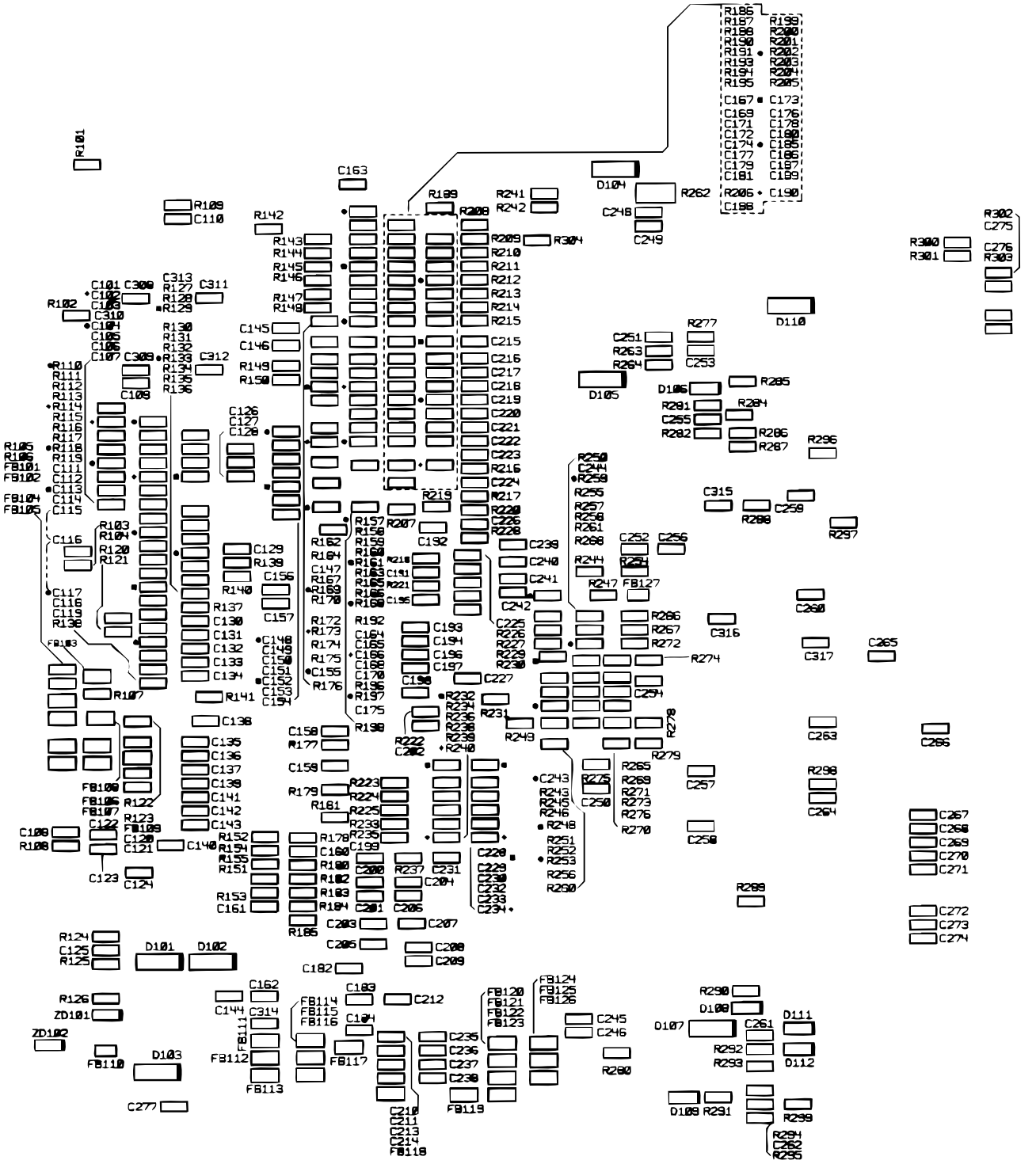

1/1
3. REAR DISPLAY PWB
DP1
FIP7B13
VFD2
VFD1
SG
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
GRID1
GRID2
GRID3
GRID4
GRID5
GRID6
GRID7
COMMAP
NOT USED
JP8
JP1
CON2
VF2R
COM/AP
SF
SG
SE
SD
G6
G5
G4
CON1
-29V
G3
G2
G1
G0
ID
DP
SC
SB
SA
VF1R

CHAPTER 9. PWB LAYOUT

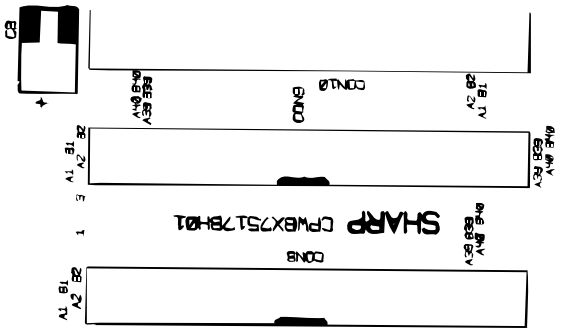
1. Main PWB (Side-A)



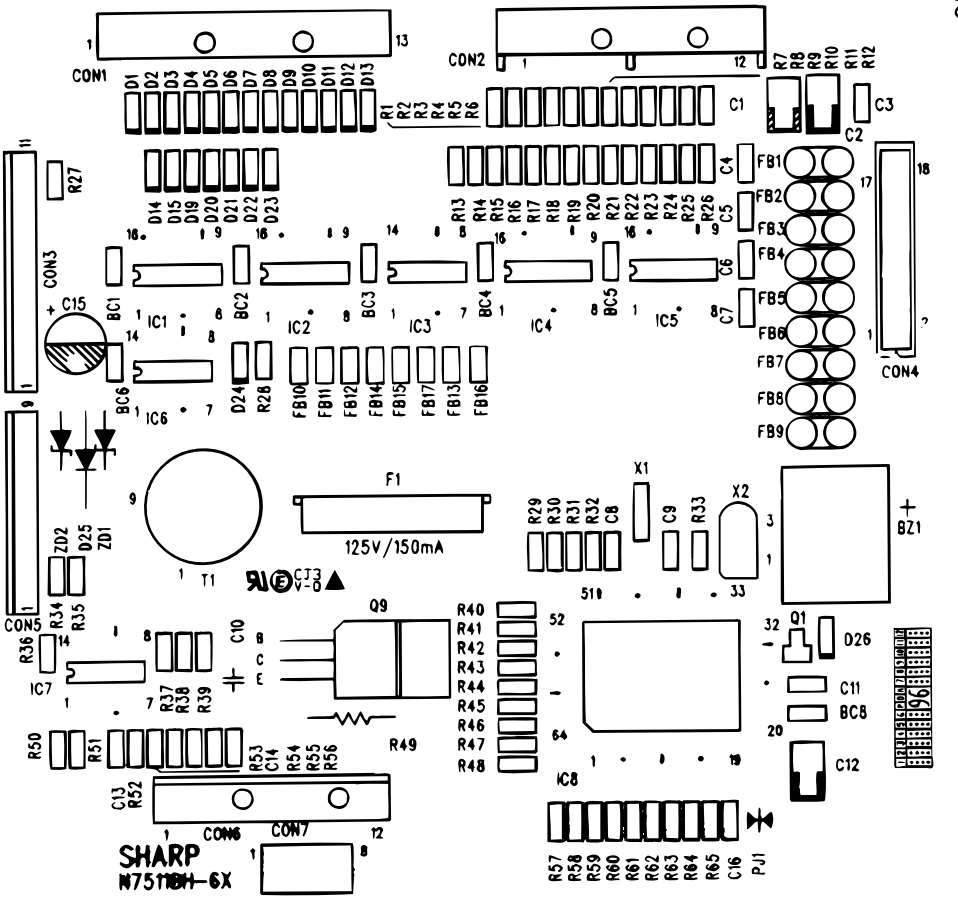
2. Main PWB (Side-B)



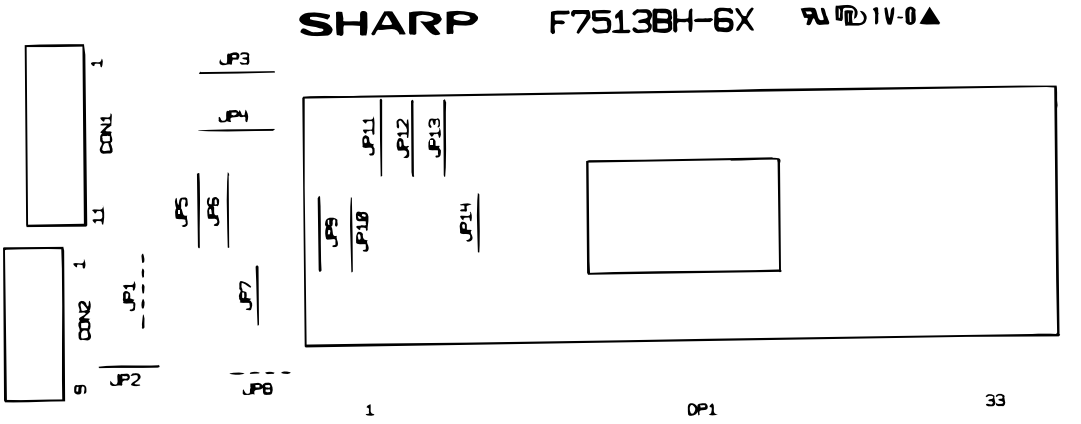
3. Mother PWB (Side-A)



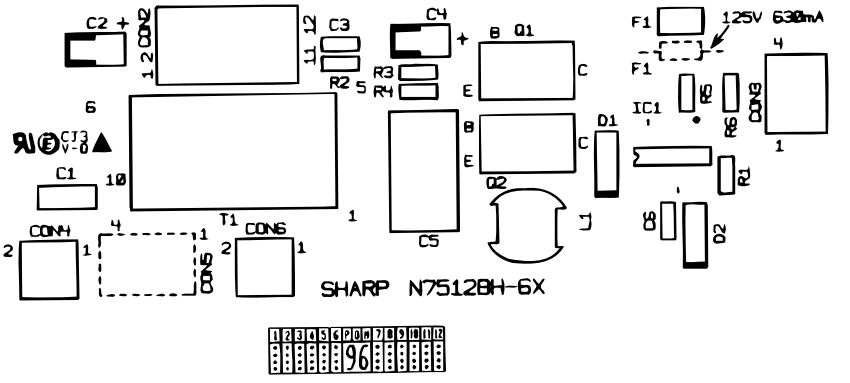
4. CKDC PWB



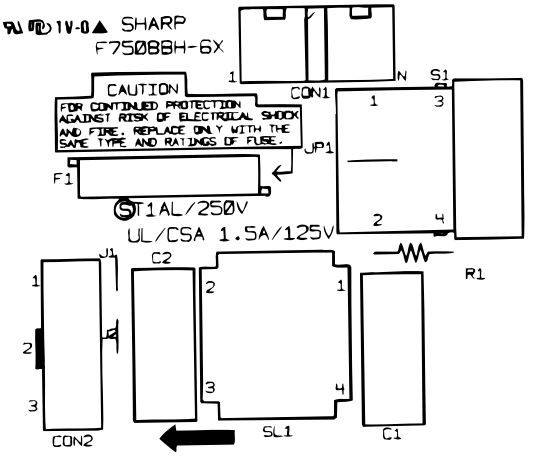
5. Rear display PWB



6. Invator PWB



7. Noise filter PWB



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